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# Prototyping of Indian Electronic Voting Machine

*-A step towards ASIC in voting*

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***Abstract:*** *The Voting System of a country consists of certain regulations which define how the preference of people is collected and how outcome of the polling process is indicating the will of people. To implement such a system in the largest democracy in the world is a cumbersome task. An indigenous Electronic Voting Machine was introduced by the Election Commission of India to overcome the issues with manual voting which was slower and inefficient. In this paper the Indian Electronic Voting Machine's Protocol for voting is implemented on a field programmable gate array. The ASIC based design is known to be faster than a microcontroller based design. Furthermore the use of an ASIC based design will make the Electronic Voting Machine a more reliable and tamper resistant machine. The new Voter-verified paper audit trail (VVPAT) system could also be interfaced with the ASIC based design. The protocol of Indian Electronic Voting Machine has been successfully implemented on a Basys 2 board using Verilog HDL. The FPGA based implementation gets half the job done for ASIC based EVM. The tool used for simulation and implementation is Xilinx ISE Design Suite with ISim as a Simulator.*

***Keywords:-*** *Prototyping, Indian Electronic Voting Machine, Verilog HDL, FPGA, Application Specific Integrated Circuit .*

## I. INTRODUCTION

Electronic Voting Machine ("EVM") is being used in Indian elections for House of the People (Lok Sabha) and State Assembly Elections (Vidhan Sabha) in the whole country since 2004. It increases voting efficiency by reducing the time in casting and counting of vote. Earlier, there were issues regarding EVM's security which have not been proved **[3]** . The claim of tampering the EVM was only relevant if and only if prolonged access to the EVM is provided by the responsible authorities or forced access is staged. However such misfortunate event is highly unlikely. Moreover tampering the machines on such a high scale is a very difficult task. The Voter-verified paper audit trail (VVPAT) system was introduced in some constituencies in Indian General Election, 2014. The Election Commission of India originated the Indian EVM with the help of two companies, the Electronics Corporation of India (ECIL) and Bharat Electronics Limited (BEL)**[1].** The Indian EVM consists of two units – Control Unit and Balloting Unit. *Control Unit*: Control Unit contains the main circuit board which consists of a Renesas H8/3644-series microcontroller driven by an 8.8672 MHz crystal oscillator, buttons for input, a buzzer, two redundant EEPROM chips and a Seven Segment Display Board and connector for the Balloting Unit **[3]**. The Election Software is permanently fused in an Internal Mask ROM in order to preserve the EVM's software from alteration.

***Ballot Unit*:** Ballot Unit consists of sixteen buttons for respective candidates. It uses two electronically programmable logic devices to communicate with the Control Unit Board. Control Unit and Ballot Unit are connected with a 5 m long cable.

**Fig. 1** Control Unit (right) and Ballot Unit (left) in the Indian EVM **[3]**.

The protocol of the aforesaid EVM is implemented using Verilog HDL. The protocol necessarily means the Input-Output responses, capabilities and procedure to use. However the ASIC based design presented here can differ in many aspects as input names, data representation during operation, memory type and Input Output Methods.

**Some key features of ASIC based EVM are:**

1. The machine can take up to 2048 votes for a single candidate and in total 8192 votes.
2. Built in self testing mechanism which checks the machine for any tampering or malicious behavior before start of voting process.
3. Candidate set switches sets the number of push buttons to be activated for the voting process.
4. The EVM makes sure that a voter has a chance to cast only one vote. No person can cast multiple votes. This is done by the blocking mechanism (10s) which is provided in the machine.
5. The EVM waits for mode and control input to be appropriately set before any vote to be casted.
6. The machine will not respond to multiple inputs to the push button for any type of malicious effort. The machine will only receive input if only one push button is pressed.
7. After the completion of voting, the mode button is turned down (output mode) and the EVM cannot reverse back to input state in any condition after that.

The Control Unit and Ballot Unit are implemented on a single FPGA board. However, proper hardware implementation of the design can result into a similar operation as that of the Indian EVM. The rest of the paper is organized as follows. Section II presents the analogy between the Indian EVM and ASIC based EVM. Section III describes the implementation and module description. Section IV shows the RTL Schematic and Waveform of the implementation. Section V describes the procedure to use. Section VI gives the future scope for the ASIC based EVM. Section VII and VIII presents the conclusion and references of the paper. In this paper the Indian Electronic Voting Machine is referred as Indian EVM.

## II. Analogy Between Indian EVM And ASIC Based EVM

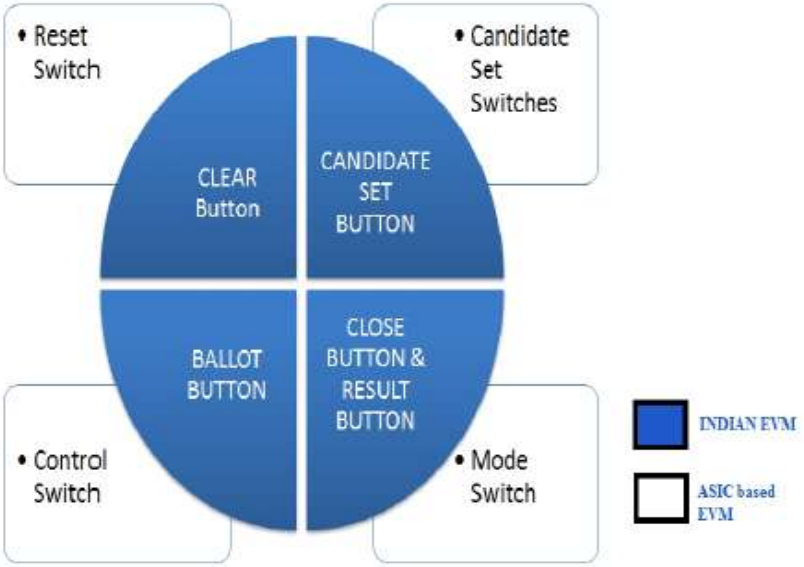


**Fig.2** Analogy between the Indian EVM and ASIC based EVM.

This paper proposes the use of an ASIC based EVM instead of a microcontroller based design in the Indian EVM. The ASIC based design provides better security features, lighter weight and a more compact design of EVM. The idea of using an ASIC based design is also supported by the fact that the original design for the EVM which was presented in 1980 by M. B. Haneefa was by using Integrated Circuits**[7]**. The design created in this paper reflects the protocol of Indian EVM. The design when implemented on FPGA will work as a prototype for testing the ASIC based design. The hardware description language used for behavioural description of the design is Verilog HDL. The approach used for designing the EVM is a combination of top-down and bottom-up. The functionality of Indian EVM is represented by several modules in its behavioural description. The proposed EVM has a single common synchronous reset which has been well defined in all the modules. There is a single common clock which is used in all the modules. The clock frequency used from the FPGA board is 50 Mhz.All the modules are described below

**1. TOP EVM:**

TOP Evm is the top module of the design. All other modules are instantiated inside the top module. This top module is synthesized, implemented and then converted into the bit file required for implementation of the design on FPGA. This bit file is then dumped on the FPGA to make it work like a prototype of the Indian EVM.

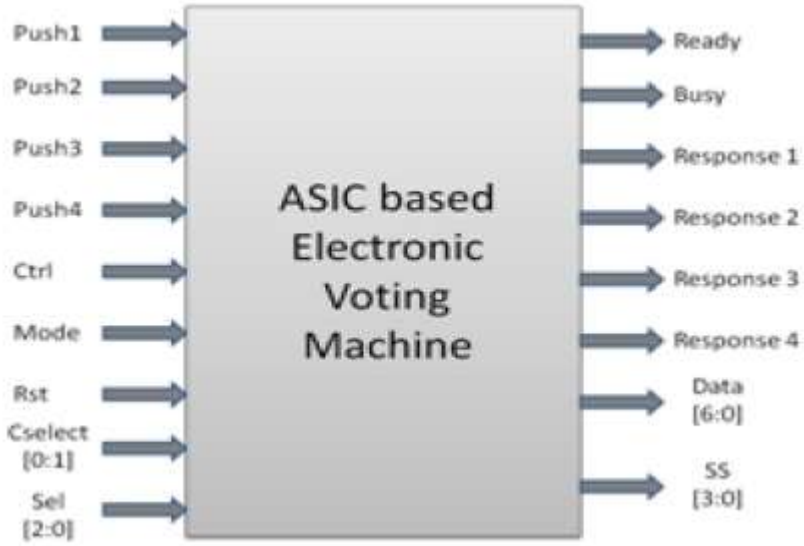


**Fig.3** Top level block diagram of ASIC based EVM

**2. FSM EVM:**

The FSM is the heart of the ASIC based EVM. The FSM is implemented using the two block method. One always block in the FSM is sequential in nature while the other one is purely combinational.

**It has the following features:**

**a.** Takes appropriate input; that is the machine will increment only one vote even if the push button is pressed several times or the push button is pressed for too long.
**b.** Masks the vote counting states that are not required for voting according to candidate select inputs.
**c.** The FSM will not take any value for input if more than one push button is pressed. There is no priority given to any push button during multiple inputs. The FSM will simply wait for the casting of a legitimate vote and will not count any vote.
**d.** Controls the ready and busy signals.
**e.** Provides the response corresponding to the respective input for a particular vote. This part could also be used to interface devices like VVPAT in future.
**f.** Checks if the mode and control of the EVM are appropriate for casting a vote, if not, the machine will remain in a blocked state.
**g.** It also controls the permission required for casting a vote that is the Control input. If the control input is not high the FSM will not be ready to take the vote. FSM will wait for the control to be high so that the vote could be casted.
**h.** If the mode is toggled once from input to output the machine will automatically seal and will not allow any further input in the respective session. The machine can renew its voting capabilities when the machine is reset.
**i.** The security features of the EVM are also incorporated in the FSM. The functionality of the Control and Mode input are also defined in the FSM_Evm module.
**j.** The increment of votes after casting of a regular vote is also handled by FSM.
**k.** After a vote has been successfully casted the machine enters into a seal state for 10s and the voter who has voted cannot do anything else on the ballot. FSM will preserve the value of the count for all the candidates for those 10s. The seal state for 10s is also administered by FSM.
**l.** The feature of preserving the value of all count for 10s also acts as a rate limiting feature for the EVM. This property of EVM can also help to reduce the damage done by malicious events like Booth Capturing.

All in all, the module FSM_Evm provides EVM the characteristics of a secure, robust, reliable, democratic and accurate machine.

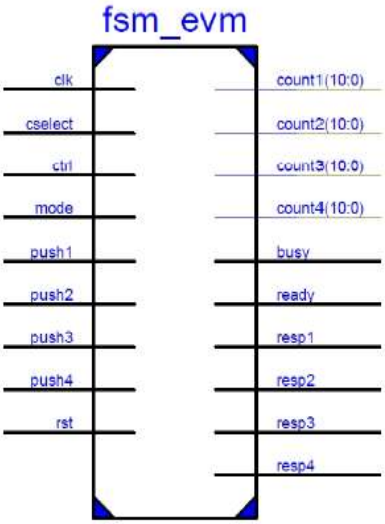


Fig.4 RTL block schematic of module fsm_evm. (Inputs on the left and Outputs on the right)

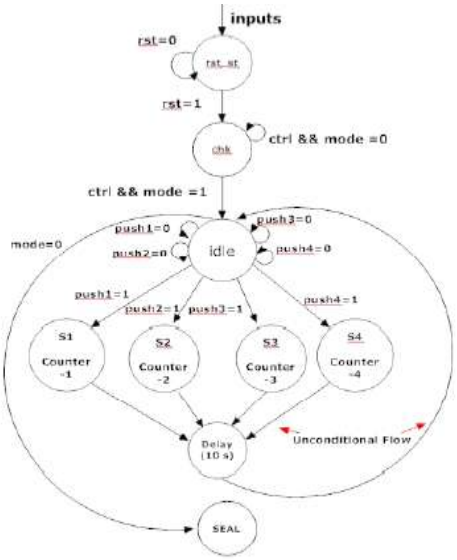


Fig. 5 Flow of control in module fsm_evm

3. **Mem countsel:**

This module is also comprised of two always blocks. Both of which are sequential in nature. The module provides the following functions. It contains memory and other selection features :

**a.** Initializing the memory so that it contains no erroneous or unknown value.
**b.** Puts the data coming from the FSM involuntarily in the memory which has been initialized.
**c.** Checks the mode and control values, so that data could be sent only when the EVM is in output mode, otherwise the data resides inside the memory.
d. Works as multiplexer to filter the data provided to the next module. As only a single value is sent to the next module depending on the value of select lines selected after the machine is put in output mode.

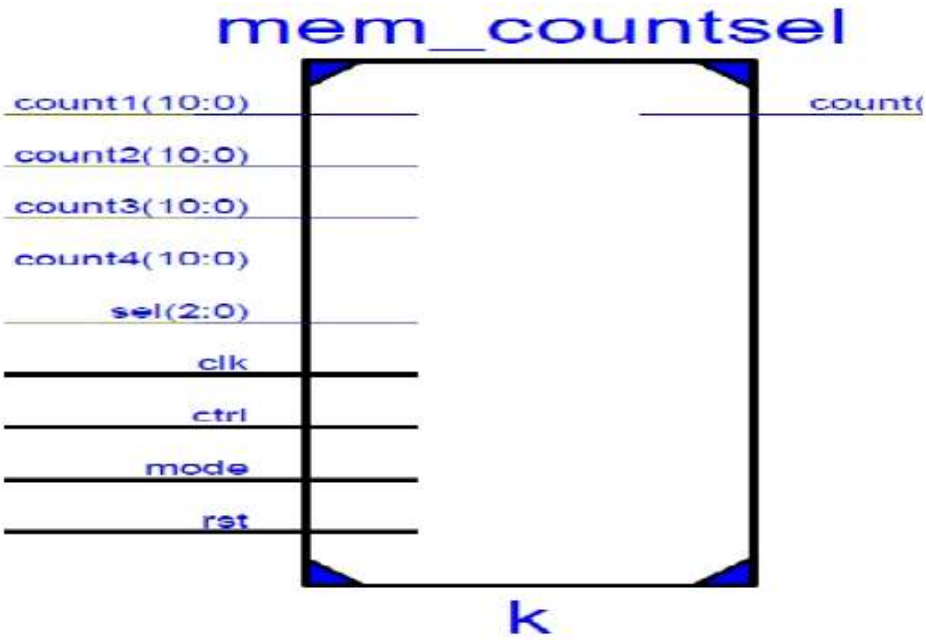


**Fig.6** RTL block schematic of module mem_countsel. (Inputs on the left Output on the right)

**4. Bin2SS :**

**The features of this module are:**

a. The module as the name suggests converts the input decimal value from the previous modules into data suitable for the seven segment display.
b. Secondly, it keeps the seven segment display off when the mode is input mode.
c. Gives four values for the four seven segments on the FPGA board.

**5. Sevensegment(CC) :**

This module is very important for displaying the data on seven segments. There are four different seven segment values coming from the previous modules. But FPGA board has only a single common data bus connected to all the Seven Segment displays. So in order to time multiplex the data bus different segments are switched at such a high rate that it a human eye cannot perceive that. It gives an illusion that all of the seven segments are working simultaneously. But in reality only one seven segment is ON at a time. The rate at which all the displays are switched is 4ms. It changes the value in all the segments after an interval of 4 ms which creates the appropriate illusion.

## IV. PROCEDURE TO USE

1. Initialize the machine by setting the reset switch to low. At this point all the switches of the prototype are low position.
2. Now set the reset switch to high. The seven segment of the machine will glow showing that there are zero votes inside the memory of machine. This is according to BIST approach used for testing of machine.(See figure 8)

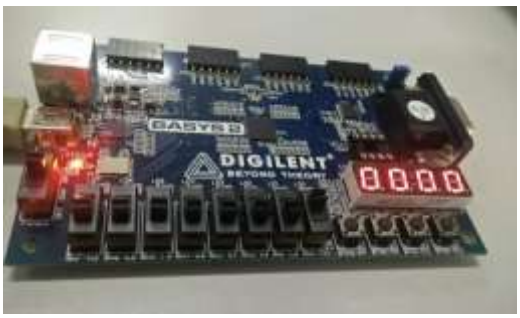


**Fig 7** Illustration of Step 2

3. The mode switch of the machine has functionality as follow:

a. Input mode – When the mode switch is at high position.
b. Output mode – When the mode switch is at low position.

As the machine has just started it have to be in Input Mode. Therefore the mode switch is set high.

4. The control switch is the switch which is controlled by the Presiding Officer when the voting is carried on. When a vote is casted, the machine generates a buzzer sound (busy led in the case of FPGA) which signals the Polling Officer to disable the machine using the control switch (low). When the next voter enters the voting area the control switch is set to high position by the Polling Officer so that the vote can be casted.

Therefore the ctrl switch is set to high so as to make the machine ready for voting.

Now, the ready led will illuminate indicating that the machine is ready to capture a vote.

5. Now, a vote is casted by a voter. As soon as the push button is pressed the machine enters into a sealed state in which the machine is blocked to take any input from anywhere in the machine. The machine will illuminate the busy led for 10s. The machine will be blocked for 10s which is ample time for the Polling Officer to set the control switch to low position. This low position on the control switch further ensures that the machine cannot take any input from the ballot even after the seal state has ended.
6. The control switch is toggled by the Polling Officer throughout the Vote casting period.(Figure 8)

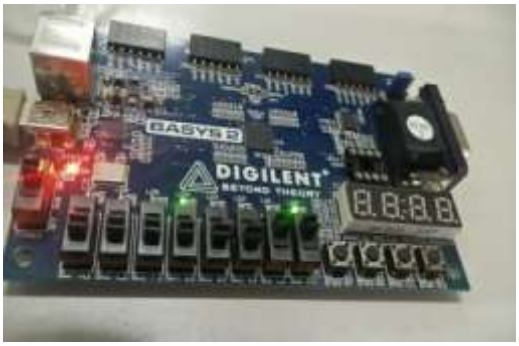


**Fig. 8** Illustration of step 6

7. Now, after the voting has been completed the mode switch is set to low position (output mode). This is a onetime step. Machine when once entered in the output mode cannot switch back to the input mode. The machine will not accept any vote in any case whatsoever.
8. Select the appropriate select lines in the form of switches that are provided for select lines. The seven segments will show the votes according to the selected candidate in the select lines or total votes. (Figure 9)


**Fig. 9** Illustration of step 8

## V. FUTURE SCOPE

The replacement of microcontroller based design with an ASIC based design for better features is definitely the best future role this idea can anchor.

1. The authentication could be extended to another level (first level with VOTER ID) using biometric security, so that one can reduce the number of polling agents required and prevent casting vote by unauthorized voters(Kumar & Begum, 2012).
2. The addition of network capabilities in the EVM could facilitate the voting process for the voters. Voters could vote from any place having internet connectivity. But such a feature should only be added if there is complete assurance regarding the network security.
3. The EVM has to be designed for larger population so that elections in the entire country could be held in a single day(Kumar & Begum, 2012).

## VI. CONCLUSION

The protocol of Indian EVM has been successfully implemented on FPGA. The prototype is working as per specifications. Some additional features are also added in the original design. The prototype has been thoroughly tested and can be used in a real Indian election if required. Dissimilarity from the Indian EVM is that the control unit and ballot are two different components in the Indian EVM but in the prototype of ASIC based EVM both units are implemented on a single FPGA board.

Rather than these dissimilarities, the ASIC based EVM works very efficiently and could easily mould to be used in a Real Indian Election.

The advantages of an ASIC based EVM are:

1. More secure than Indian EVM. Difficult to crack.
2. Compact design.
3. More economical.
4. Lighter weight than Indian EVM.

## VII. RTL SCHEMATIC AND WAVEFORM

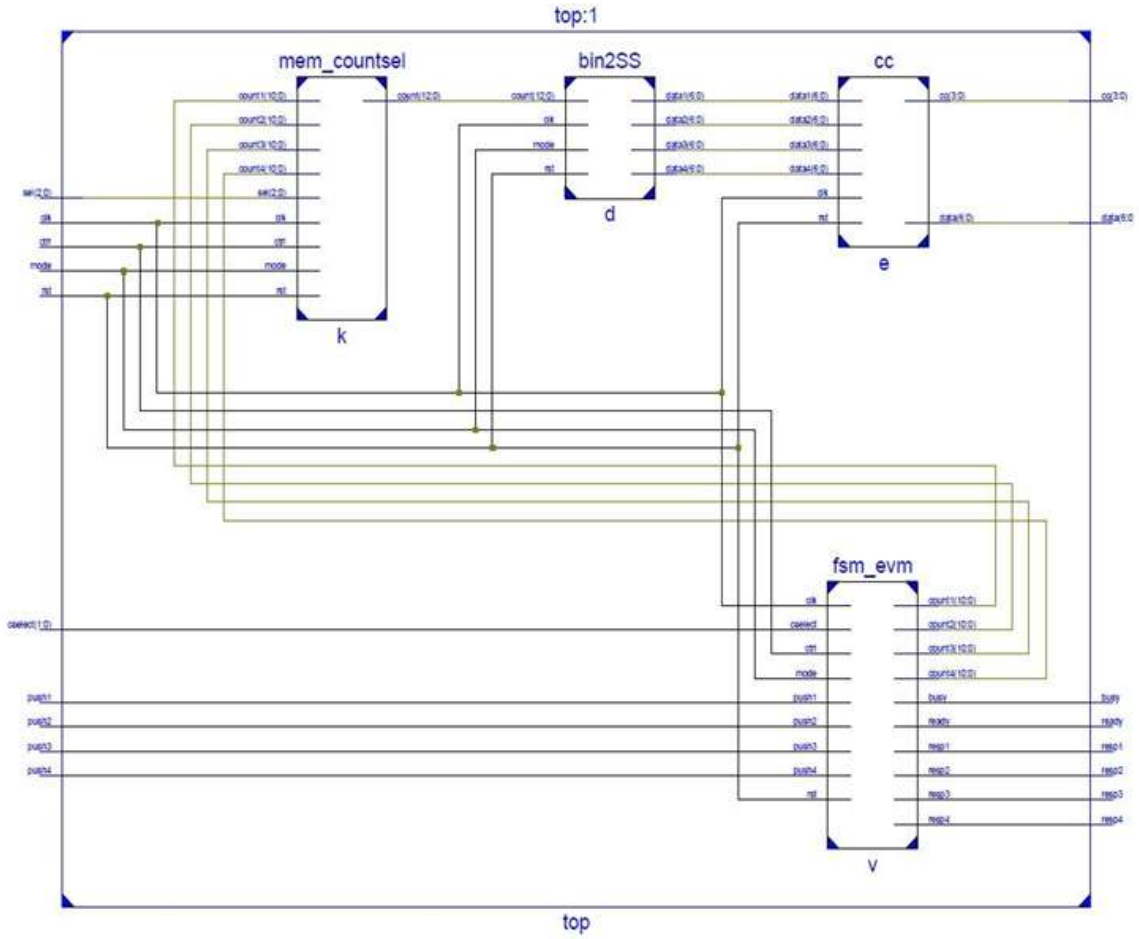


**Fig. 10** RTLschematic of the ASIC based EVM

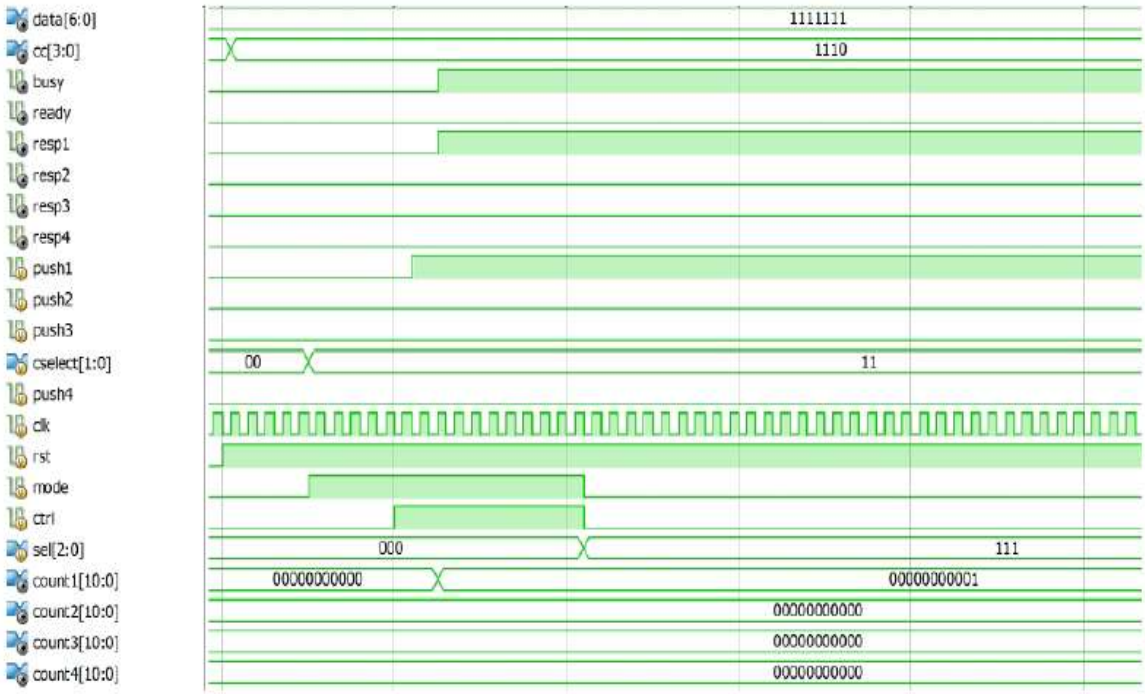


**Fig. 11** Simulation Waveforms showing vote casted by candidate 1.

## REFRENCES


[1]. *Public Notice :PN/ECI/41/2009* INDIA, Election Commission of India(2009). Electronic Voting Machines-regarding.

[2]. D. Ashok Kumar and T. Ummal Sariba Begum "**Electronic voting machine — A review**" Pattern Recognition, Informatics and Medical Engineering (**PRIME**), 2012,**IEEE Conference 21-23 March 2012**

[3]. Hari K. Prasad , J. Alex Halderman , Rop Gonggrijp , "**Security Analysis of India's Electronic Voting Machines**" appeared in **Proc. 17th ACM Conference on Computer and Communications Security , July 2010**

[4]. Sahibzada Muhammad Ali, Chaudhary Arshad Mehmood,Ahsan Khawja, "**Micro-Controller Based Smart Electronic Voting Machine System**" IEEE Conference 21-22 March 2013

[5]. Davide Balzarotti, Greg Banks, Marco Cova,"**An Experience in Testing the Security of Real-World Electronic Voting Systems"** IEEE Transactions On Software Engineering, Vol. 36, No. 4, July/August 2010

[6]. **Handbook for presiding officers,** 2008.

[7]. http://eci.nic.in/eci_main/ElectoralLaws/HandBooks/Handbook_for_Presiding_Officers.pdf

[8]. **From Wikipedia, the free encyclopedia, the web page on Indian EVM** https://en.wikipedia.org/wiki/Electronic_voting_in_India