International Journal of Engineering Research and Development
e-ISSN: 2278-067X, p-ISSN: 2278-800X, www.ijerd.com
Volume 8, Issue 2 (August 2013), PP.76-81

Design of Dual Port SDRAM Controller with Time Slot Register

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Abstract:- The main purpose of this paper is to verify the SDRAM controller data transfer function when accessing data from multiple ports. This verification is done with memory testers using slot mechanism.

Random data sent to SDRAM from two ports, one port at a time. The SDRAM controller reads data from two random generators through different memory testers.

SDRAM controller writes data in to SDRAM, and then read data and send to concerned memory tester. Compare the read and write data in Memory testers.
A Dual port module is added with SDRAM controller, to switch data accessing from port alternately.

Index terms:- Dualport, Slot timing, Switching operation and Comparing Read/write data.

I. INTRODUCTION

Functional simulation of dual port SDRAM controller mainly consists of 4 modules Random data generator, Memory tester, Dual port and SDRAM controller.

A. *Random data generator*

It is a 16-bit serial data generator in which data that is produced changes for every clock; this is achieved by XOR'ing the Outputs of last four flip flops and is feedback as the input to the first flip-flop.

B. *Memory tester*

Memory testers are used to compared the written data and read data to/from SDRAM. Its working depends upon the pipelined operation or non-pipelined operation. In pipelined operation all the data from the given range of address which is read and written are compared whereas for non-pipelined operation data in given address is compares individually, if there is any mismatch between the read and written data it indicates an error.

C. *Dual port Module*

This design is used to select any one of the two ports at a time. The data read follows the same bus as written and activated port is shown as the status.

D. *SDRAM Controller*

SDRAM controller accepts simple read and write requests on the host-side and generates the timed waveforms required to perform these operations on the SDRAM. With pipelining enabled, read and write operations within a row of the SDRAM can be dispatched for every clock cycle. The controller also manages the refresh operations needed to keep the SDRAM data valid, and will place the SDRAM in a self-refresh mode so data is retained even if the controller ceases operation.

Controller works on the master clock of 133 MHz. The cycles related to initialization cycles, RAS (Row address strobe) cycles, RCD (activation to read/write) cycles, refresh cycles, mode cycles, CAS (column address strobe) cycles are specific for given RAM. The Micron soft module SDRAM (MT48LC16M16A2 – 4 Meg x 16 x 4 banks) is used here.

BLOCK DIAGRAM

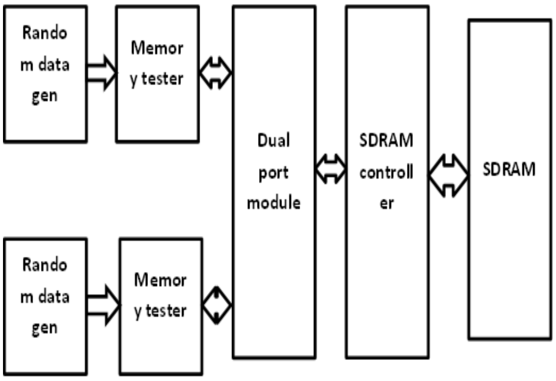


Fig1. Functional simulation of dualport SDRAMcontroller.

II. RANDOMDATA GENERATOR

The random data generator generates a random 16 bit data using a shift registers.

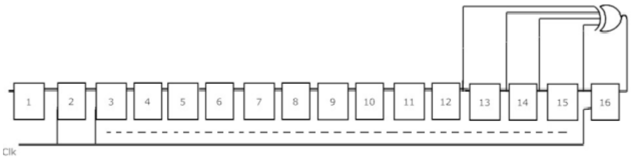


Fig2. Random data Generator

To go through the sequence of states for the register, it is assumed that the shift register is in the seed state and the random output starts from that seed state and changes for every clock.

The maximum number of states it can have with four stages shift register. So this sequence is called the maximum length sequence (MLS) and is given by 2^n -1. Where n is the number of stages in the shift register. Enter a given clock frequency, the periodicity of the randomness increases rapidly with the number of stages of the register increases.

The circuit shown in fig2 for generate a 16-bit random data, in this, the output from 12,13,14,15 stages of left shift register is XORed and feed as input to 16th stage of shift register.

Table1. Random generator output values

Clock	Output Data
Clk-1	Seed– FFFF
2	FFFE
3	FFFC
4	FFF8
5	FFF0
6	FFE0
7	FFC0
8	FF80
9	FF00
10	FE00
11	FC00
12	F800
…	…….
….	…….
…..	…….
…..	…….

III. DUAL PORT MODULE

The dual port module is used to select any one of the two ports, either port0 or port1. Data will be accessed from any of two ports, divide the total memory in to two memory slots.

The address and data is directed to port activated at that slot, so that read and write operation will be initiated or started from that port.

16-bit Time-slot allocation register is used to switch between port0, port1. If address register content is 1111111111110000(for 16 bit address),the Port0 will be activated for four clock cyclles, then port1 activates for remaining 12 clock cycles.

Different signals of the ports are indicated in the following diagram.

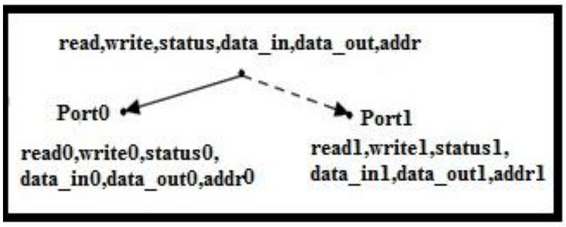


Fig3. Dualport signals

The possible operations of dual port module

Case1: Switching operation

Switching is occurs if a read or write operation is requested on this port that is not currently active:

- No R/W operation is being performed on the active port or
- A R/W operation is in progress on the active port, but the time-slot allocation register is giving precedence to the inactive port.
- It indicates when an operation on the active port is in-progress and can't be interrupted by a switch to the other port.

Case2: Slot timing

Update the time-slot allocation shift-register. The port with priority is indicated by the least-significant bit of the register. The register is rotated right if:

- The current R/W operation has started.
- Both ports are requesting R/W operations (indicating contention), and
- The currently active port matches the port that currently has priority.
- Under these conditions, the current time slot port allocation has been used so the shift register is rotated right to bring the next port time-slot allocation bit into play.

Case3: Port activation in next cycle

The active port is switched on

- There are no pending operations in progress, and
- The currently active port has finished its current R/W operation
- The port switch indicator is active.

Case4: Port management with gate

Gate is open for the active port to initiate new R/W operations to the SDRAM controller.

If any port request for R/W operation, when any operations are in progress with other port, gate is closed to prevent R/W operations from requested port.

The gate is re-opened once all operations in progress are completed, at that time the switch to other port is indicated, it can issue its R/W commands.

IV. MEMORY TESTER

This module is required along with Random data generator to test the data that has been read and written. The data that is generated is first given to memory tester through dualport module, it is written into SDRAM using SDRAM controller and dual port module.

In order to write/read the data it is required to check whether it is a pipelined or non-pipelined operation. In case of pipelined operation, it writes the data into all the addresses specified at a time and for non-pipelined the data will be written location by location.

The entire operation is divided into 5-states as

- Initialization
- Load
- Compare
- Empty pipe
- stop

Initialization: In this state the read and write are disabled before going to further states and the starting address is loaded into the address variable. Then it goes to next state i.e. load.

Load: First it looks for non-pipelined or pipelined operation. For pipelined operation the write operation is enabled and if operation has begun then addr-variable is incremented till the end address is reached and then data is written into SDRAM.

Whereas for non-pipelined data is written, address by address which is incremented in steps to reach the end address by checking whether previous write operation is done.

Compare: Written data in SDRAM is compare with read data from SDRAM. In case of pipeline operation the comparison takes place at once. In case of non-pipeline operation the comparison will be done location by location. If the data is not as written data, then it is indicated as an error.

Empty Pipe: In pipelined operation, if there are no read/write operations, it clears the pipeline. If any operation is pending it waits till it is completed.

Stop: At the end of memory testing operation it stops. If the comparison has to repeat starting from initialization then repeat the process. The entire memory testing operation can be represented in a form of a state diagram as Pipeline Operation

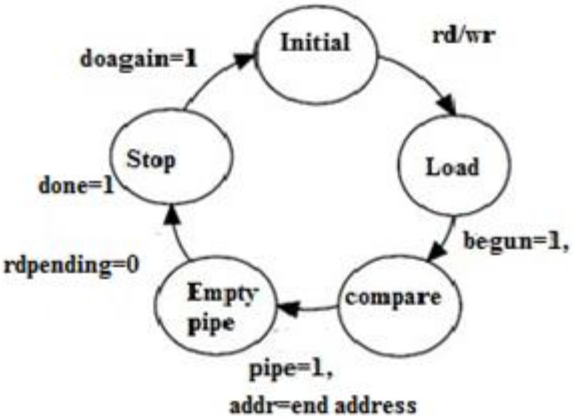


Fig4. Pipeline operation.

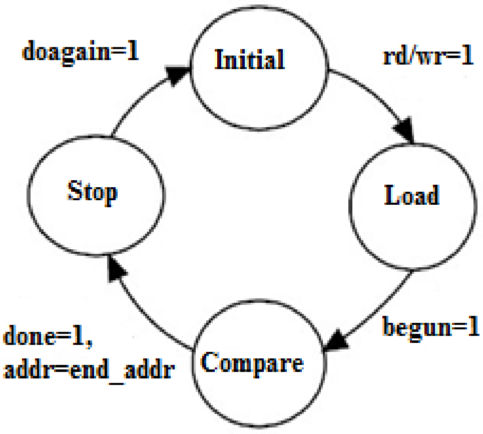
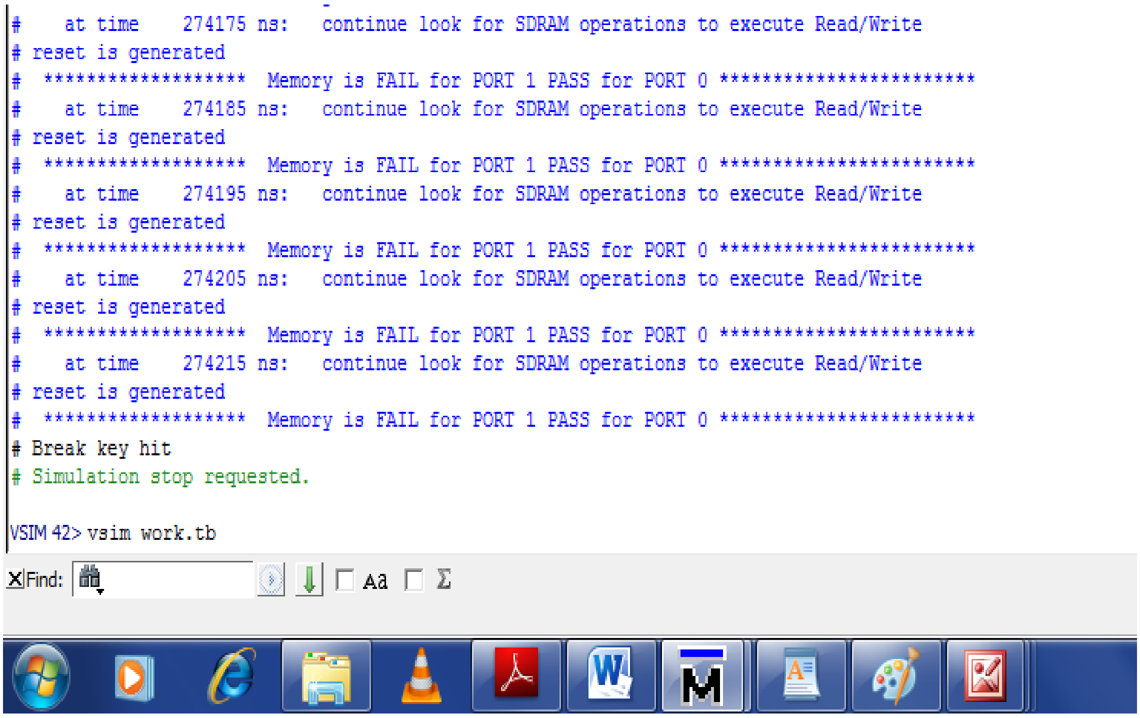


Fig5. Non-pipeline operation.

V. SIMULATION RESULTS

In simulation of dual port SDRAM controller, port 0 and port 1 are reading and writing data separately from different memory testers using slot mechanism. In simulation see the output k is 1 and 0 gives respective ports 1 and 0.



```
#    at time    274175 ns:   continue look for SDRAM operations to execute Read/Write
# reset is generated
#  *******************  Memory is FAIL for PORT 1 PASS for PORT 0 ************************
#    at time    274185 ns:   continue look for SDRAM operations to execute Read/Write
# reset is generated
#  *******************  Memory is FAIL for PORT 1 PASS for PORT 0 ************************
#    at time    274195 ns:   continue look for SDRAM operations to execute Read/Write
# reset is generated
#  *******************  Memory is FAIL for PORT 1 PASS for PORT 0 ************************
#    at time    274205 ns:   continue look for SDRAM operations to execute Read/Write
# reset is generated
#  *******************  Memory is FAIL for PORT 1 PASS for PORT 0 ************************
#    at time    274215 ns:   continue look for SDRAM operations to execute Read/Write
# reset is generated
#  *******************  Memory is FAIL for PORT 1 PASS for PORT 0 ************************
# Break key hit
# Simulation stop requested.

VSIM 42> vsim work.tb
```

Fig6. Output

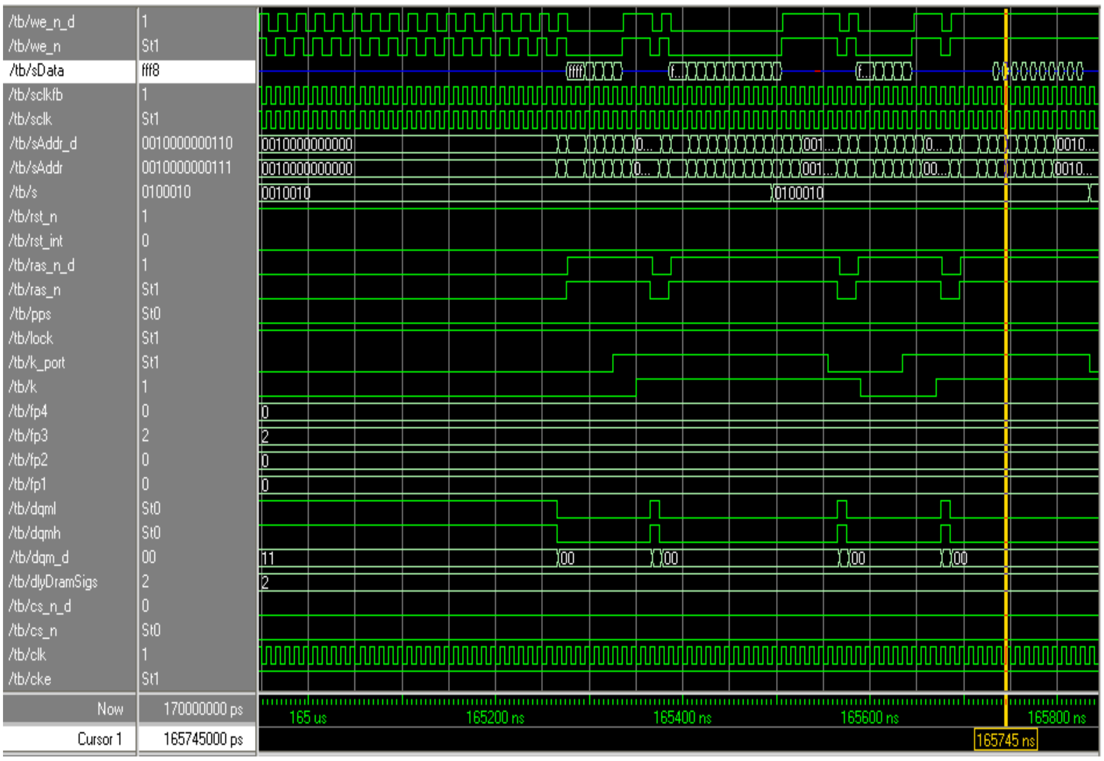


Fig7.Output Data for corresponding address

VI. CONCLUSION

In this design switching of two ports can done manually depend on bits provided in generic 16-bit Timeslot register.

Upgrade this paper to multiport, by dividing address locations into multiple slots and accessing these multiple ports using provided value in 16-bit Timeslot register.

Here two different modules instead of memory testers to continuously send data and loaded in to SDRAM from two ports.

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