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Operational Transconductance Amplifier for Highly Linear Application

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Abstract*—This paper presents a highly linear Operational Transconductance Amplifier (OTA) that combines two linearization techniques, one with adaptive biasing of differential pairs and second with resistive source degeneration. The Operational Transconductance Amplifier has ±0.9v power supply. Operational Transconductance Amplifier has been simulated with TANNER 0.18µm CMOS technology in Tspice. The simulated third order harmonic distortion (HD3) with applying a 300mvP-P differential input, remains below -60dB at 3MHz frequency which gives coefficient of correlation(R^2) 0.9892.

***Keywords*— Operational Transconductance Amplifier (OTA); linearity; adaptive bias circuit; source degeneration.**

I. INTRODUCTION

Operational Transconductance Amplifier (OTA) is a fundamental building block of analog circuits and systems. OTA has been used to implement many kinds of analog circuits such as; operational amplifier, data converters, four-quadrant multipliers, mixers, modulators and continuous-time filters [1]-[10]. In such application as asymmetrical digital subscriber lines (ADSL) and cable-modem, the linearity has to be 60dB while for example, video applications require at least 60dB of linearity at 5MHz [5]. Gm-C topology is a good choice for realizing continuous-time filter has better performance in frequency response and electronic tuning capability, but suffer from poor linearity[5], [8]. Thus designing an OTA with high linearity tends to be a constraint in circuits and systems design task.

In literatures several techniques have been presented to design linear transconductor blocks. In [3] utilizing a tail current depends on the square of input differential signal, linearity in output current of strong inversion transconductor has been improved. This technique which is known as adaptive bias technique loses its performance due to second order effects in modern nano scale devices. Source/gate degeneration is another technique for linearity enhancement, specially in nano scale CMOS technology which the HD3 due to mobility reduction effect is considerable [2]. Some other techniques use two or multiple Gm cell to cancel third order harmonic distortion [4], [9]. Double Differential Pair (DDP) is one of these techniques that uses two cross coupled differential pairs. Then choosing proper size and tail current biases can cancel the third order harmonic. The main drawback of these techniques is higher power consumption and transconductance loss [4]. In this paper we combine both adaptive bias [12] and source degeneration techniques to improve the linearity of a transconductor. A well accurate-precise analog processing requires a pure wanted signal. This means that the required signal is distortion free and interference free (common mode signal). Consequently to ensure the best processing condition high linear signal. the point which seems to be less regarded in most works so far. Therefore in this work the adaptive bias circuitry is improved to provide a l high linearity. In section II we propose the principle and theoretical relations of these linearization techniques. In section III complete linear OTA is shown. In section IV simulation results are given and in section V we conclude the paper.

II. PRINCIPLE OF LINEAR TRANSCONDUCTOR

Fig. 1 shows a source-coupled n-channel differential pair that is biased by current tail *ISS*. In this figure *vin1* and *vin2* are input signals including both common and differential modes. The large-signal i-v transfer characteristic will be given by:

$$Iout = I_{D1} - I_{D2} = \frac{1}{2}\beta v_{in}\sqrt{\frac{4Iss}{\beta} - vin^2} \quad |V_{in}| \le \sqrt{\frac{2Iss}{\beta}} \qquad (1-a)$$

$$I_{D1} - I_{D2} = I_{ss}\ \mathrm{sgn}(vin) \qquad |V_{in}| > \sqrt{\frac{2Iss}{\beta}} \qquad (1-b)$$

$$\beta = \mu_n C_{ox}\frac{W}{L}, \qquad v_{in} = v_{in1} - v_{in2}$$

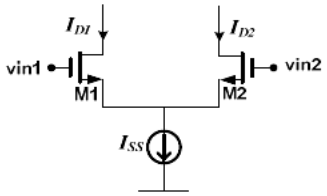


Fig. 1 Simple Differential Pair

In equation (1) *Vin* is differential input (*vin1-vin2*) and "sgn" is sign function. Other parameters in (1) have their usual meanings. For realizing a linear relation between differential output current and differential input voltage, the result of radical in (1-a) should be a constant. This will be realized using a tail current containing a component dependent on the quadratic input vin^2 to cancel the nonlinearity of the output current. So assuming $I_{ss} = I_{ss0} + k'V_{in}^2$ we get:

$$Iout = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}\sqrt{\frac{4Iss0}{\beta\mu n\ cox\ W/L} + \left(\frac{4k'}{\mu n\ cox\ W/L} - 1\right)} \qquad (2)$$

In [12] biasing current, dependent to input signal has been implemented with cross coupled differential pair biased by constant separate current source. Fig. 2 shows the improved adaptive biased transconductor. In Fig. 2, the currents of M5, M6 transistors can be expressed as follows [4]:

$$I_5 = I + I - \Upsilon\left(V_{in}\sqrt{K/I}\right)^2 + \frac{x}{2}\left(V_{in}\sqrt{K/I}\sqrt{1-\eta\left(Vin\sqrt{K/I}\right)2}\right. \qquad (3\text{-a})$$

$$I_5 = I + I - \Upsilon\left(V_{in}\sqrt{K/I}\right)^2 + \frac{x}{2}\left(V_{in}\sqrt{K/I}\sqrt{1-\eta\left(Vin\sqrt{K/I}\right)2}\right. \qquad (3\text{-b})$$

Where,

$$x = 4n/(n+1), c\ \eta = n/(n+1)2\ ,\ \Upsilon = n(n-1)/(n+1)2$$

$$K = \frac{1}{2}\mu_n c_{ox}\frac{W}{L} \qquad (4)$$

Sum of these currents depends on the quadratic input vin^2 As :

$$I5 + I6 = 2I + 2I\ -\Upsilon\left(V_{in}\sqrt{K/I}\right)^2 = 2I + 2n(n-1)/(n+1)^2\ KV_{in}^2 \qquad (5)$$

Which is the same as $I_{ss} = I_{ss0} + k'V_{in}^2$ if

$K' = \left[2n(n-1)/(n+1)^2\ K\right]$ To remove the nonlinearity in (2) we should have [5]:

$$\frac{4k'}{\mu_n C_{ox} W/L} - 1 = 0 \Rightarrow \frac{2k'}{k} - 1 = 0 \Rightarrow k' = \frac{k}{2}\ ,n = 2.155 \qquad (6)$$

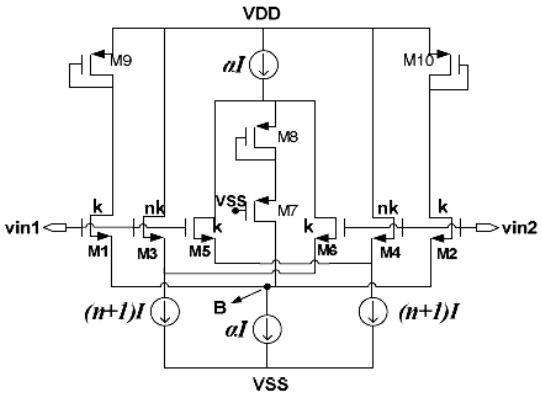


Figure 2. Improved version of adaptive biased transconductor

For short channel devices the effective carrier mobility is a function of both the longitudinal and transversal electric fields. Considering the degradation of mobility due to these effects the drain current of a transistor in saturation region can be approximated as [11]:

$$I = \frac{k(VGS-Vth)2}{1+\theta(VGS-Vth)}\ (1+\lambda VDS) \qquad (7)$$

Where, θ is the mobility reduction factor. From (7) The effect of θ can be interpreted as the use of a degeneration resistance of value $R\theta = \theta / 2k$ connected to source terminal. In Fig. 2, mobility reduction effect results in a tail current which depends also on forth power of input signal as equation (8)[12].

$$I_{ss} = I_{ss0} + k' V_{in}^{\ 2} + k'^{3}\, Req^2 V_{in}^{\ 4}$$
$$Req = \frac{\theta n}{2kn} + \frac{\theta p}{2kp}$$

(8) Equation (8) shows that mobility reduction effect degrades the capability of adaptive bias technique in linearity improvement. Thus, for linearity improvement in this work, we use both adaptive bias and source degeneration techniques. For simplicity we investigate the effect of source degeneration technique for decreasing HD3 in a simple differential pair. Ignoring second order effect, the output current of Fig. 1 can be described by a Taylor series expansion as follows:

$$iout = ID1\text{-}ID2 = \sum_{n=0}^{\infty} GM,(2n+1)vin^{2n+1} \qquad (9)$$

Where, GMs are the coefficients of odd powers of the differential input voltage. Considering mobility degradation effect we will have:

$$GM,1 = \frac{1}{2}\ \frac{\sqrt{kp\left(\frac{W}{L}\right)Iss}}{1+\frac{2}{\varepsilon crit}\sqrt{\mathrm{Iss}/\mathrm{WLKp}}} \qquad (10\text{-}a)$$

$$GM,3 = -\frac{GM,1}{8\left(\frac{Iss\ L}{2Kp\ W}\right)\left(1+\frac{2}{\varepsilon crit}\sqrt{Iss/WLKp}\right)3} \qquad (10\text{-}b)$$

Where K_p is a technological parameter, $\varepsilon crit$ is the critical electric field, W is the width and L is the length of the transistors[5]. If two source degeneration resistors be added as shown in Fig. 3, the ac components of the output approximately becomes:

$$\mathrm{iout} = \frac{GM,1}{(1+GM,1R)}vin + \frac{1GN,3}{(1+GM,1R)4}\mathrm{vin}^3 \qquad (11)$$

Relation (11) shows that HD3 is decreased by 1 (1+ $N\ r$)3, where $Nr = GM,1R$. Using this topology for source degeneration (two resistors that current tail is in middle of them) has lower input referred voltage noise.

III. PROPOSED OTA

With reference to principles explained in section II the complete fully differential OTA which benefits from the source degeneration and adaptive bias techniques shown in Fig. 4. In this circuit α=4, n=2.16, I=20μA and ICSS=10μA. To avoid from drawbacks associated with resistive source degeneration which mentioned before, small resistors (R=210Ω) is used.

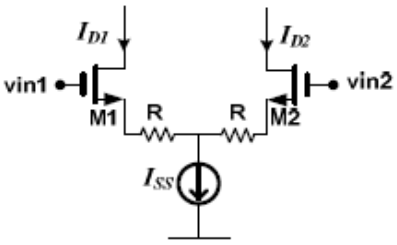


Figure 3. Source degeneration for linearity enhancement.

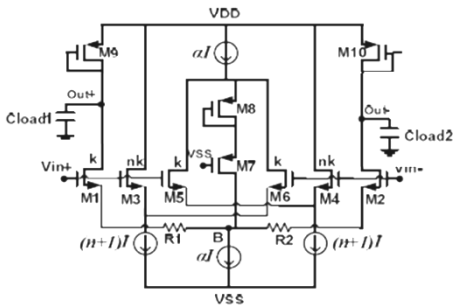
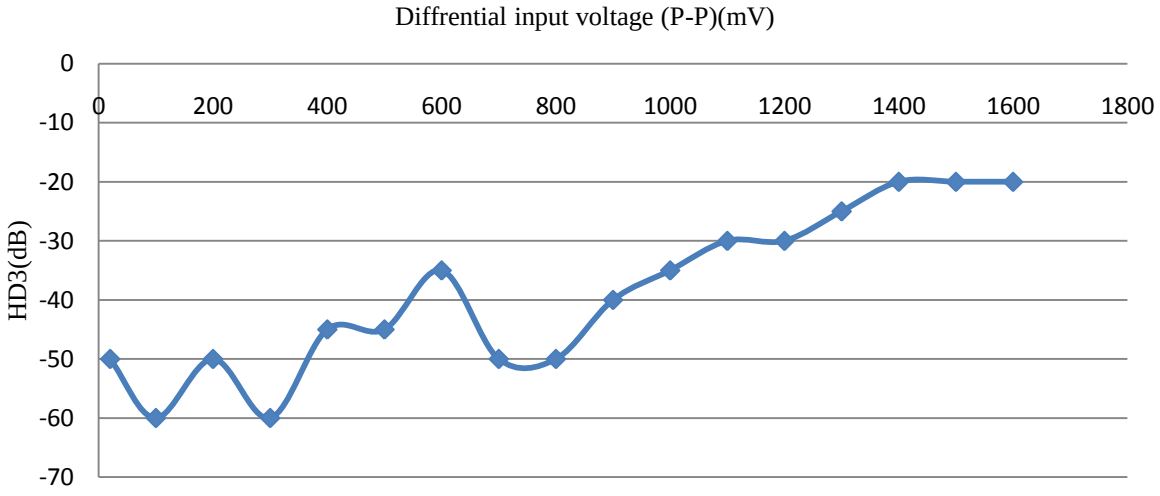


Figure. 4 Proposed linear OTA.

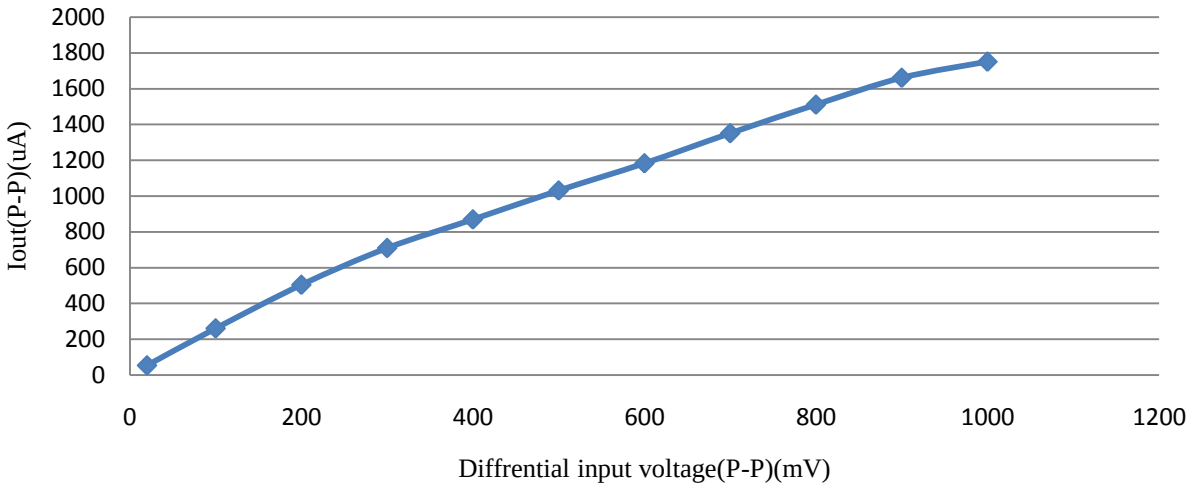
The simulation result show that improved version of adaptive bias circuit and source degeneration circuit provide linearity with coefficient of corelation (R^2) =0 .9894.

IV. SIMULATION RESULTS

The proposed OTA (Figure 4) have been simulated using the standard 0.18µm CMOS technology in Tspice simulator. Power supply of the circuit is ±0.9v. Applying an input signal with frequency near to unity gain frequency (3MHz), HD3 of output current in capacitance loads verses magnitude of input signal with source degeneration and adaptive bias technique is shown in . In figure 5-b the value of peak-to-peak differential current in capacitance loads (iCload1-iCload2) is also shown. Table I shows the main specifications of proposed OTA compared with some similar works.



(a)



(b)

Figure 5. (a) HD3 of output current using adaptive bias technique and source degeneration with R= 210Ω. (b) Peak to Peak differential output current with coefficient of correlation(R^2) = =0 .9892.

Table I. **SPECIFICATIONS OF PROPOSED OTA COMPARED WITH SIMILAR WORKS.**

Specification	**This work**	**[15]**	**[9]**	**[10]**
Technology	0.18um	0.18um	0.18um	0.18um
Supply voltage	0.9V	1V	1.8V	1.1V

DC gain	45dB	NA	NA	63dB
Transconductance	43uA/V	100 uA/V	20 uA/V	NA
Linearity	HD3= -60 dB 0.3Vp-p at 3MHz	HD3= -55dB 0.7V p-p at 30MHz	HD3= -65 dB 0.6Vp-p at 1MHz	THD= -62 dB 1Vp-p at 100KHz

V. CONCLUSION

In this paper we have proposed a highly linear OTA which combines two linearization techniques. An improved Adaptive bias circuitry and source degeneration with low resistance (210Ω) is utilized to improve the linearity in nano scale CMOS technology. Using small resistors makes this circuit suitable for low voltage low-power application. OTA has been simulated with 0.18μm CMOS technology in Tspice. The simulated third order harmonic distortion (HD3) with a 300mvP-P differential input remains below -60dB for frequency up to 3MHz which gives coefficient of correlation(R^2) = 0 .9892.

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