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Design of High-Speed Dynamic Double-Tail Comparator

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ABSTRACT:- The analog-to-digital converters which are of ultra low-power, area efficient, and high speed converters are made of dynamic regenerative comparators. These comparators can maximize speed and power efficiency. The delay and power dissipation of dynamic comparators are analyzed in this paper. The delays and tradeoff can be explored. The circuit of a conventional double tail comparator in this analysis is modified for fast operation even in different supply voltages. By using power gating technique and adding few transistors, the positive feedback during the regeneration is strengthened in the proposed comparator structure. The delay time can be reduced by providing positive feedback instead of adding few transistors. The analysis results are going to be confirmed on the basis of 0.25-µm CMOS technology. The power consumption and delay time can be significantly reduced based on this analysis. All the simulation are made using TANNER TOOLS, Generic 250nm. The schematic are drawn in the T-SPICE schematic editor.

Keywords:- Double-tail comparator, high-speed analog-to-digital converters (ADCs), delays, low-power analog design.

I. INTRODUCTION

The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison. Comparators are known as 1-bit analog to digital converter and for that reason they are mostly used in large abundance in A/D converter. The basic comparator consists of three blocks. The first stage is the preamplifier, followed by a positive feedback or decision stage, and an output buffer. The preamplifier stage amplifies the input signal to improve the comparator sensitivity i.e. it increases the input signal by which the comparator can make a decision and isolates the input of the comparator from switching noise which comes from the decision stage. This is used to determine which of the input signals is large. The output buffer amplifies the information and gives a digital output signal Designing of high-speed comparators in CMOS technologies with low supply voltages is difficult because of threshold voltages of the devices is also small that cannot be scaled [3]. Therefore, designing of high-speed comparators is highly difficult for the smaller supply voltages.

There are many techniques to amplify the supply voltages, such as supply boosting methods[2],[9], techniques employing body-driven transistors[5],[12], current-mode design method[8] and by using dual-oxide processes. These techniques can handle higher supply voltages that have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques which are used to increase the supply voltage, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but the drawback is that they introduce reliability issues in CMOS technologies. The threshold voltage requirement can be eliminated in body-driven technique [5] because MOSFET operates as a depletion region [12].

A comprehensive analysis about the delay of dynamic comparators has been presented for various architectures in this paper. The different structures of double tail comparators are designed and analyzed in 250nm technology of Tanner tools by providing a supply voltage of 5V. A new dynamic comparator is presented based on the double-tail structure proposed because it does not require boosted voltage or stacking of too many transistors. The latch delay time is profoundly reduced by adding a few minimum-size transistors to conventional double-tail dynamic comparator. Designing of proposed double-tail dynamic comparator is based on separation of inputs with cross coupled stage [7]. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

I. CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. The comprehensive delay analysis is presented in which the delay time of three common structures, i.e. conventional dynamic comparator,

conventional dynamic double-tail comparator and modified double tail comparator are analyzed, based on which the proposed comparator will be presented.

A. Conventional Dynamic Comparator:

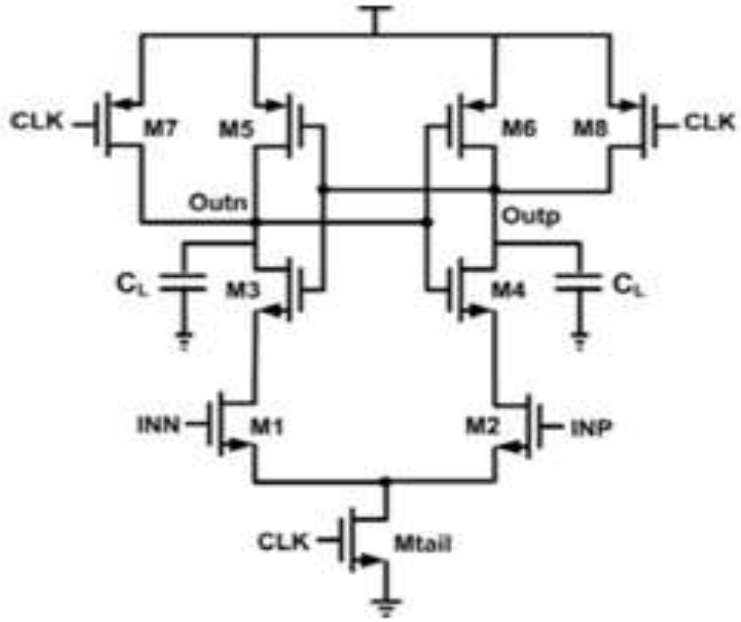

Fig1. Circuit diagram of conventional dynamic comparator.

The Circuit diagram of conventional dynamic comparator is shown in figure1. The conventional dynamic comparators are widely used in A\D converters because of having high input impedance, good rail-to-rail output swing and no static power consumption [3]. These comparators have good robustness against noise and mismatch [3].

Operation of conventional dynamic comparator:

When the clk=0(reset phase) the transistor Mtail will be in off state and PMOS transistor M7,M8 are in on state then the terminals Outn, Outp are pulled to VDD. When the clk=VDD (comparison phase) the transistor Mtail will be in on state and PMOS transistor M7,M8 are in off state then the terminals Outn, Outp that are already pulled to VDD Start discharging from VDD. The comparison of inputs can be shown based on different discharging rates of outn and outp terminals. If the VINP is greater than VINN, then Outp discharges faster than outn. When Outp terminal reaches to the voltage VDD-|Vthp| then the PMOS transistor M5 becomes on and provides a path to pull Outn to VDD and Outp terminal completely discharges. If the VINP is less than VINN, then Outn discharges faster than outp. When Outn terminal reaches to VDD-|Vthp| then the PMOS transistor M6 becomes on and provides a path to pull Outp to VDD and Outn terminal completely discharges. If the input VINP and VINN are equal then the discharging rates of Outp and Outn are equal. The delay of comparator consists of two time delays t0, tlatch. The delay t0 represents the capacitive discharge of load capacitance CL until the first p channel transistor (M5\M6) turns on.The delay tlatch represents the latching delay of two cross coupled inverters. The disadvantage is that, due to several stacked transistors, high supply voltage is needed to compensate the delay time. Another drawback of the structure is that there is only one current path, via tile transistor Mtail. The large tail current helps for fast regeneration of latch [7]. Transient analysis and simulation of conventional dynamic comparator is shown in figure2 whereas schematic and layout is shown in figure3 (a), (b) respectively.

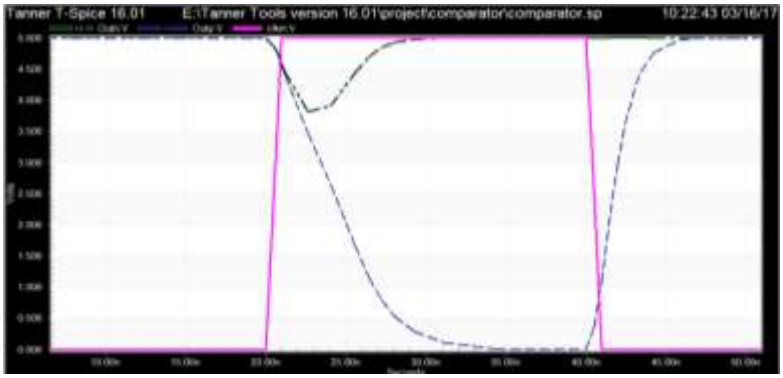

Fig2. Transient analysis of conventional dynamic comparator.

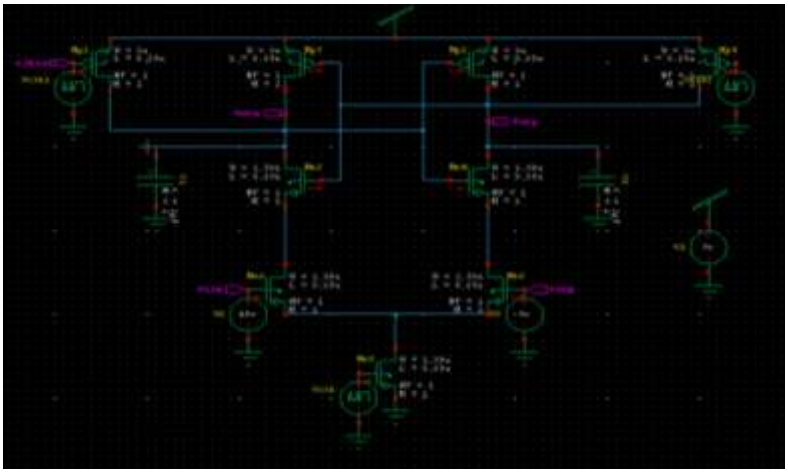

Fig3(a).Schematic of conventional dynamic comparator.

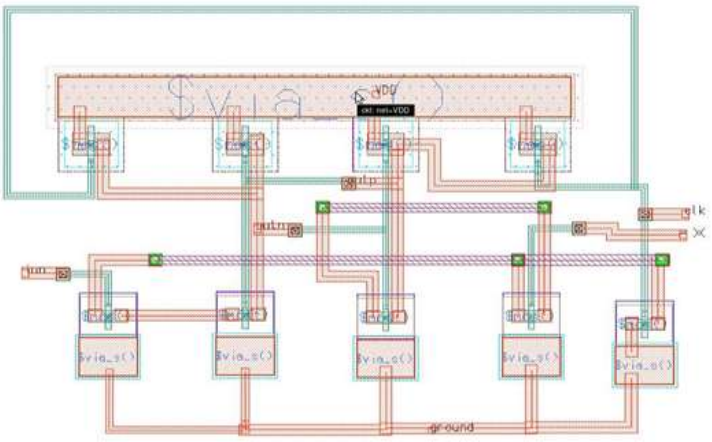

Fig3(b). Layout of conventional dynamic comparator.

B.Conventional Double-Tail Dynamic Comparator:

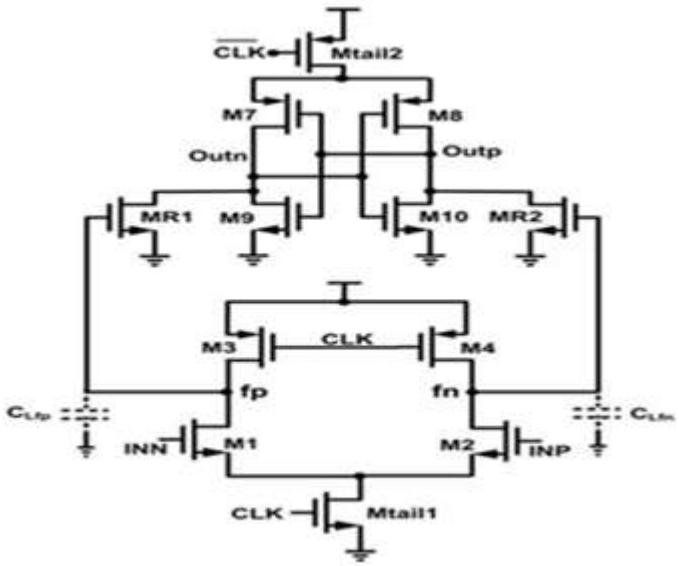

Fig4. Circuit diagram of conventional double-tail dynamic comparator.

The Circuit diagram of conventional dynamic double-tail comparator is shown in figure4. The disadvantage i.e. more stacking of transistors in conventional dynamic comparator can be overcome by using this structure. This circuit can operate at lower supply voltages compared to conventional dynamic comparator.

Operation of conventional dynamic double-tail comparator:

When the clk=0(reset phase) the transistor Mtail1 and Mtail2 will be in off state and PMOS transistor M3, M4 are in on state then the nodes fp and fn precharges to VDD which in turn causes transistor MR1 and MR2 will be in on state and discharges the output nodes to ground. When the clk=VDD(decision making phase) the transistor Mtail1 and Mtail2 will be in on state and PMOS transistor M3, M4 are in off state then the nodes fp and fn start discharging from Vdd which in turn causes transistor MR1 and MR2 will be in cutoff state and the output nodes reaches to Outn and Outp terminals. The comparison outputs for different inputs are based on different charging and discharging rates.

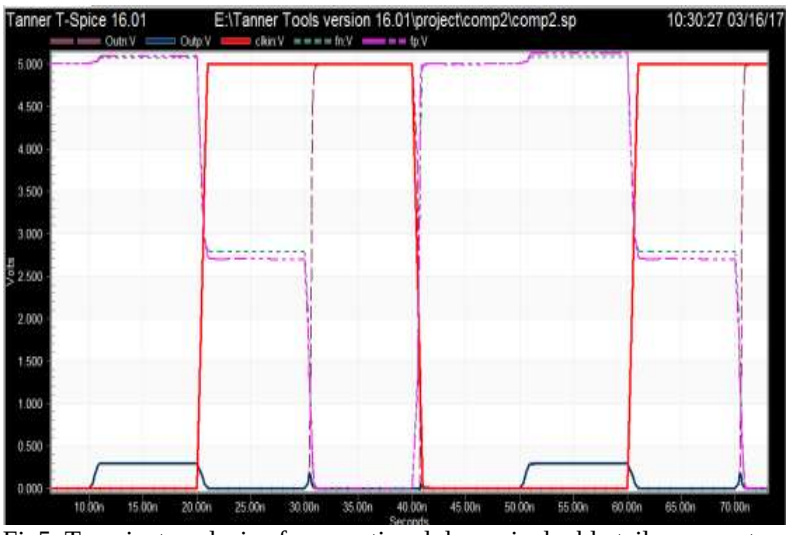

Fig5. Transient analysis of conventional dynamic double tail comparator.

Similar to conventional dynamic comparator the delay of conventional dynamic double tail comparator comprises of two main parts t0, tlatch as shown in figure4. The delay t0 represents the capacitive charging of load capacitance CL until the first n channel transistor (M9/M10) turns on. The disadvantage is that because of having double tail structure large current is required in latching stage. The schematic and layout for conventional double-tail dynamic comparator is shown in figure6(a), 6(b) respectively.

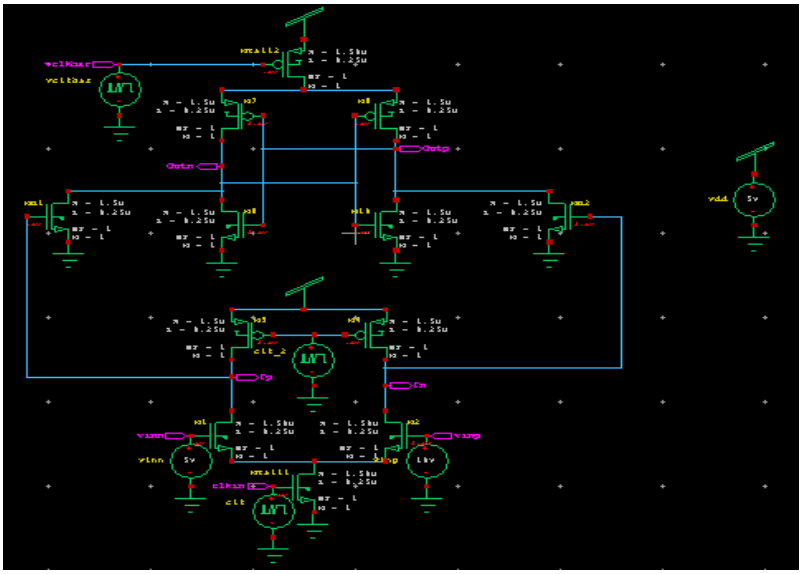

Fig6(a). Schematic of conventional dynamic double-tail comparator

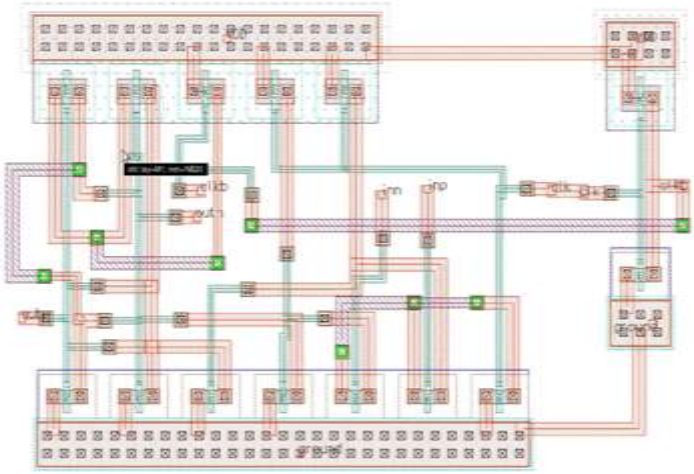

Fig6(b). Layout of conventional dynamic double-tail comparator.

C. Modified Conventional Double-Tail Dynamic Comparator Main Idea:

Figure7 demonstrates the Circuit diagram of modified dynamic double tail comparator this comparator is used to increase $V_{fn/fp}$ in order to increase latch regeneration speed. This can be achieved by using two control transistors Mc1, Mc2 added in parallel to M3, M4 transistors in cross coupled state.

Operation of modified dynamic double-tail comparator main idea:

The operation of modified double tail comparator is given below. When the clk=0(reset phase) the transistor Mtail1 and Mtail2 will be in off state and the PMOS transistors M3 and M4 will be in on state and pulls both fp and fn nodes to VDD. Hence the control transistor Mc1 and Mc2 will be in cutoff state. Then the intermediate stage transistors MR1 and MR2 will be in on state and the output resets to ground. When the clk= VDD (decision making phase) the transistor Mtail1 and Mtail2 will be in on state and the PMOS transistors M3 and M4 will be in off state. Thus fp and fn nodes start to drop with different rates according to input voltages. If VINP>VINN then fn drops faster than fp. The control transistor Mc1 and Mc2 will be still in cutoff state. Then fn and fp starts discharging. The transient analysis of this comparator is shown in figure8, schematic and layout is shown in figure9(a), 9(b) respectively.

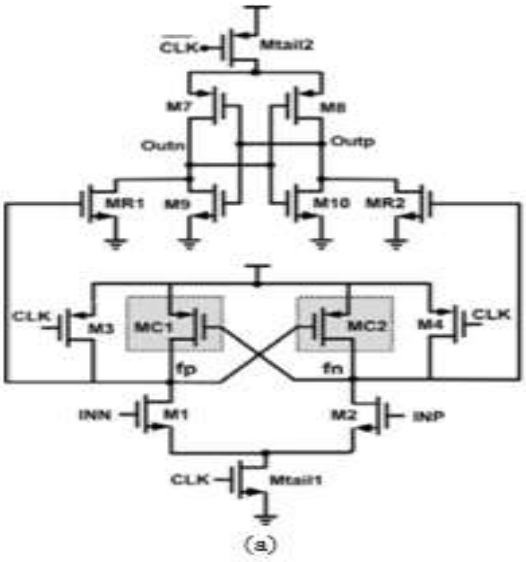

Fig7. Circuit diagram of modified double-tail dynamic comparator main idea.

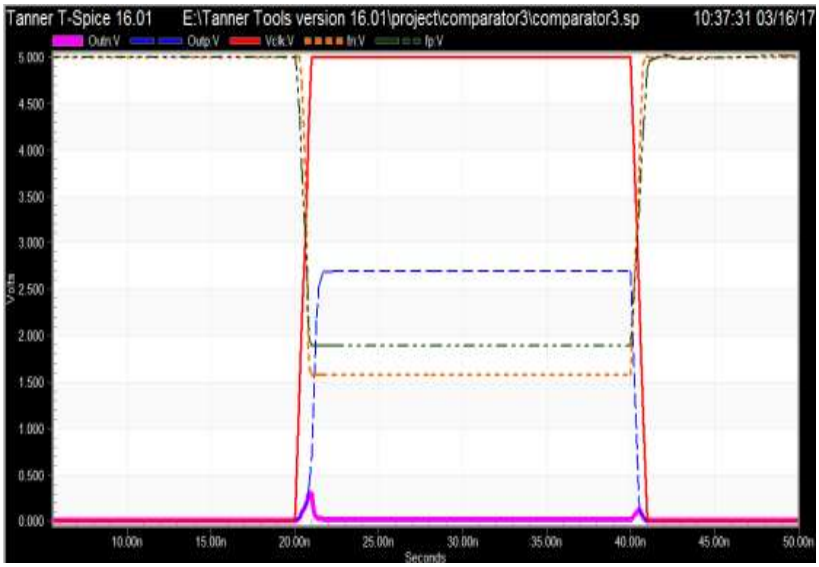

Fig8. Transient analysis of modified double-tail dynamic comparator main idea.

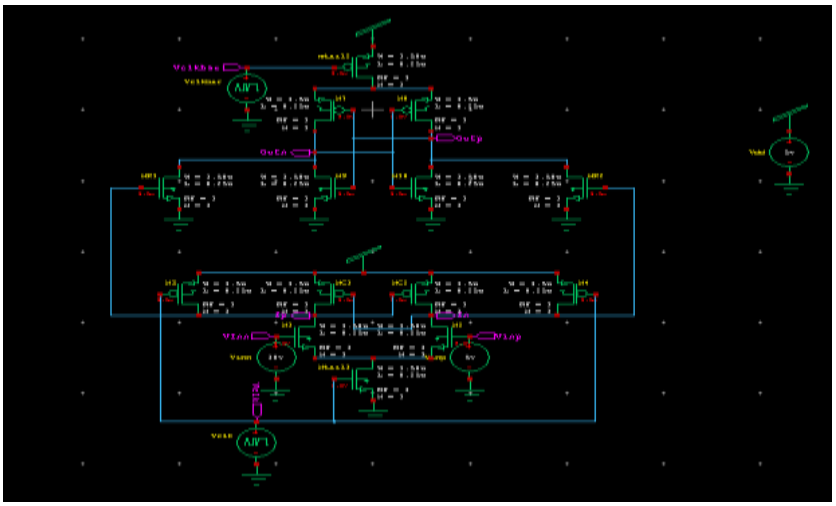

Fig9(a). Schematic of modified dynamic double-tail comparator main idea.

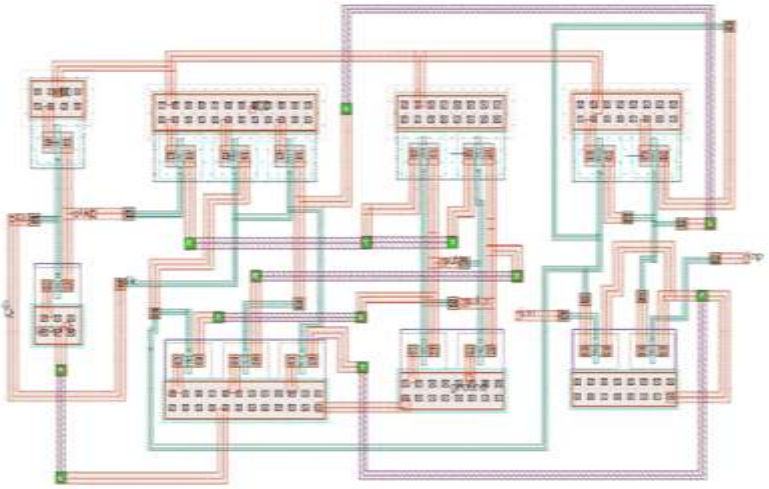

Fig9.Layout of modified dynamic double-tail comparator main idea.

D. Modified Conventional Double-Tail Dynamic Comparator Final Structure:

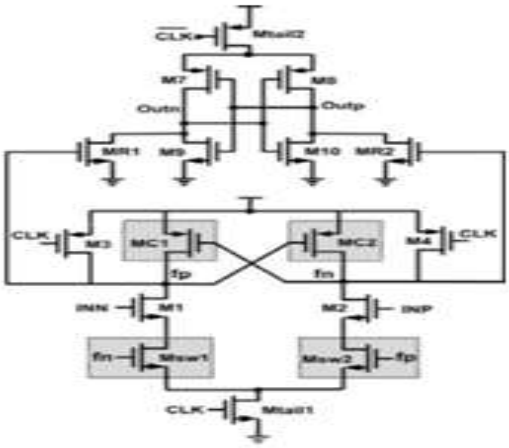

Fig10. Circuit diagram of modified double-tail dynamic comparator final structure.

The disadvantage of using the modified double tail dynamic comparator is having more static power consumption. It means that when a control transistor Mc1 and Mc2 becomes on then current from VDD is drawn to ground via input and tail transistors. In order to overcome this drawback two NMOS switches Msw1 and Msw2 are added below the input transistors which is shown in figure10.

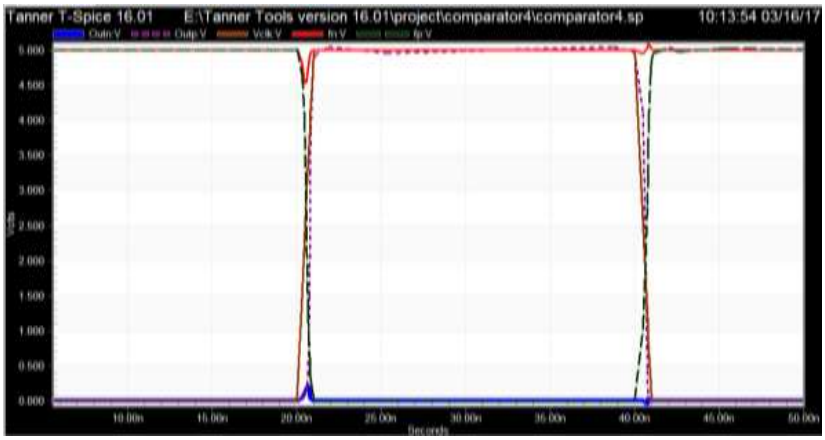

Fig11. Transient analysis of modified double-tail dynamic comparator final structure.

Operation of modified dynamic double-tail comparator final structure:

When the clk= VDD (beginning of decision making phase) the transistor Mtail1 and Mtail2 will be in on state and the PMOS transistors M3 and M4 will be in off state. Thus fp and fn nodes those are precharged to VDD start to drop with different discharging rates according to input voltages. At any case, if comparator detects that any one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase the voltage difference. The operation of control transistors with the switches emulates the operation of latch.

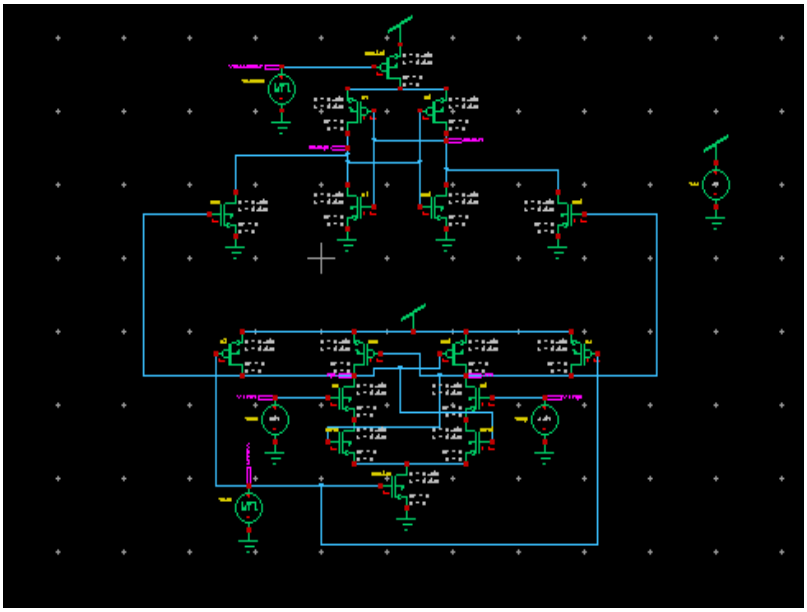

Fig12(a). Layout of modified final structure dynamic double-tail comparator.

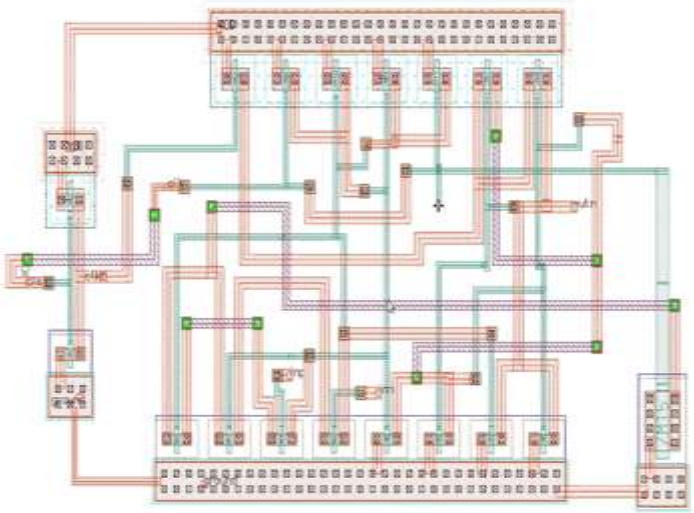

Fig12(b).Layout of modified final structure dynamic double-tail comparator.

E. Proposed Double-Tail Dynamic comparator:

Due to the better performance of double tail structure in low-voltage applications, the proposed comparator is designed based on the double tail structure. This comparator resolved clock overhead problem by replacing clk signal with fp and fn nodes. The Circuit diagram of the proposed dynamic double tail comparator is shown in the Fig.9 with two NMOS switches (Mn1 and Mn2) added to the switching transistors (Msw1 and Msw2) in order to reduce the static power consumption. This circuit works similar to the previous comparator structure.

This circuit uses the power gating technique to reduce the static power consumption. The additional transistors switches when it has high input voltage otherwise it remains in the off state and reduces power consumption by grounding the static power consumed. In addition to reducing the stand-by power, power gating has the merit of enabling testing.

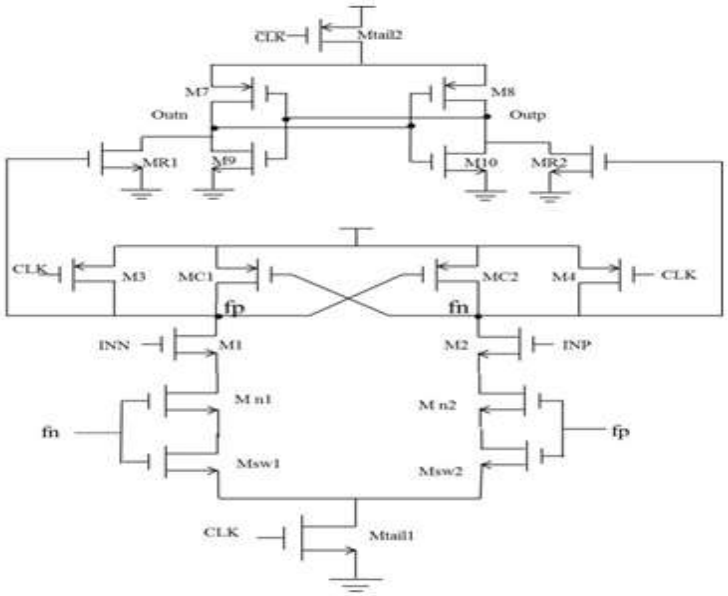

Fig13. Circuit diagram of proposed double-tail dynamic comparator.

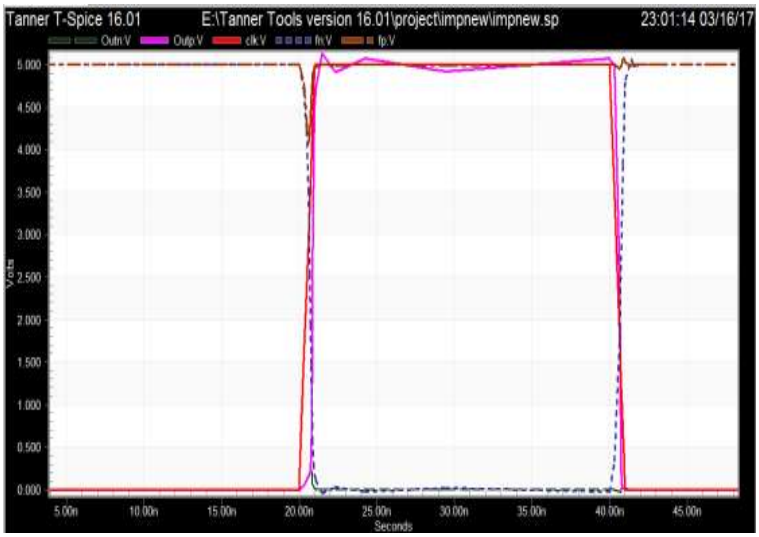

Fig14. Transient analysis of proposed double-tail dynamic comparator.

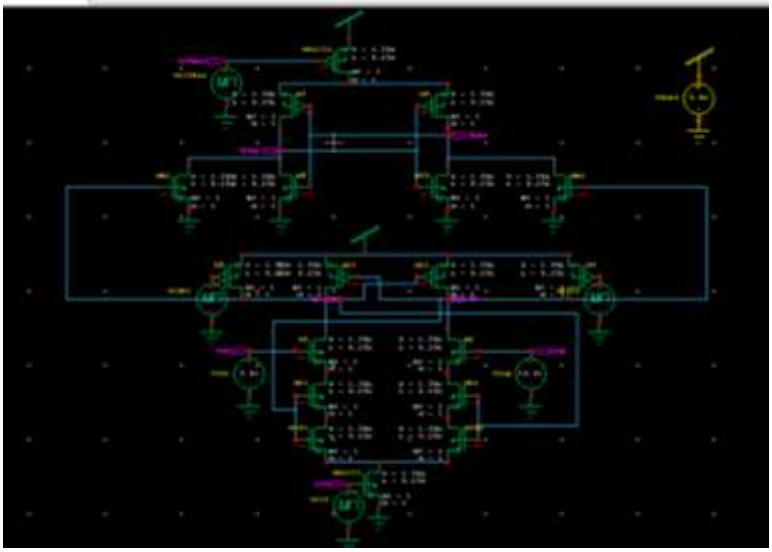

Fig15(a).Schematic of proposed double-tail comparator

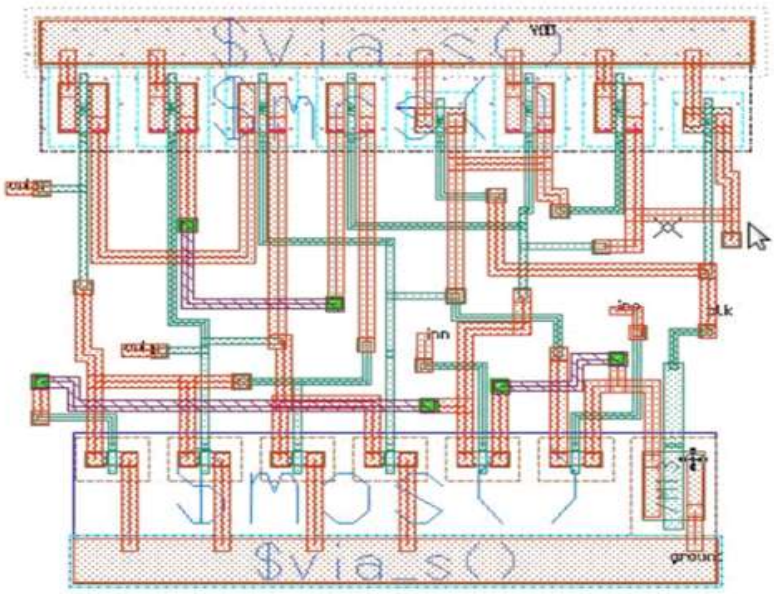

Fig15 (b). Layout of proposed double-tail comparator.

III. DESIGN CONSIDERATIONS

Some design issues that to be considering while designing the proposed comparator is that, the size of the tail transistors (Mtail1 and Mtail2) should ensure that time required for one of control transistors to become on must be smaller than t0. The control transistors should be chosen with low threshold PMOS devices in order to get turn on. While designing NMOS transistors, drain-source voltage of these switches must be considered.

IV. SIMULATION RESULTS

In order to compare the proposed comparator with the conventional, double-tail dynamic comparators and modified double-tail comparator, all circuits have been simulated in a 0.25-μm CMOS technology with V_{DD} = 5V. The layouts of modified and proposed comparators are shown in figures below.

Table I: Comparison of comparator performance**:**

Specifications	Conventional dynamic comparator	Conventional dynamic double tail comparator	Modified comparator main idea	Modified comparator final structure	Proposed double tail comparator
Technology	250nm	250nm	250nm	250nm	250nm
Supply voltage(V)	5V	5V	5V	5V	5V
N.o of transistors	9	12	14	16	18
Delay	12.725nsec	147.5667psec	19.526nsec	248.65psec	11.8342psec
Power dissipation	0.9307mW	0.3292mW	4.31mW	0.1212mW	0.13050mW

V. CONCLUSIONS

The delay and power dissipation analysis for clocked dynamic comparators were analyzed in this paper. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on those analyses, a new dynamic double tail comparator was proposed in order to improve the performance of the comparator and to overcome the clock overhead problem. Post-layout simulation results in 0.25-μm CMOS technology confirmed that the delay and energy dissipation of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator. The proposed circuit has reduced power consumption and less delay when compared to the existing comparator structure.

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