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Hardware Implementation of Fuzzy Processors: A Review

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ABSTRACT:- A review paper on the various VLSI architectures of fuzzy logic based processors and controllers is presented over here. The focus of this paper on the study of low power VLSI implementation of fuzzy processors to result in reduced silicon area, high operating speed and the adaptability to various application domains. The paper reviews the design and implementation of different components of a fuzzy logic processor, like fuzzifiers, defuzzifiers, inference engine and rule base systems. It is been found that there is a huge scope for further improvement of these components of fuzzy processor in terms of power, speed, area and complexity in these fuzzy processors. It has been found that the researchers generally focus on the design and development of inference engine and defuzzification units in a fuzzy processor due to their complex nature. The further optimization in these blocks can result in a in a significant improvement in the overall performance of the fuzzy processors.

Keywords:- Design, defuzzifiers, fuzzy logic, inference engine, low power designing.

I. INTRODUCTION

Lotfi Zadeh [1-3] is being considered as the father of fuzzy logic, as it is he who has given the concept around four decades before. Since then the fuzzy logic has been used in numerous applications and in every domain of science and technology. The fuzzy logic has been extensively used control engineering, consumer electronics, house hold appliances, data processing, decision making systems, expert and signal processing systems and so on. A biggest advantage of the fuzzy logic is the easy modelling of human behaviour; it directly maps the human inference system to the fuzzy *if – then* rules, which are easily understood by the human beings [4-6]. Fuzzy logic has been used extensively in the field of medical science [7-8], Y. C. Yeh *et al.* [7] proposed a simple fuzzy system to study electrocardiogram (ECG) to determine heart beats in human beings. The rapid growth in the applications of fuzzy systems has provided enough motivation to researchers to design efficient fuzzy systems [8-12].

The classical way to realize a fuzzy system is to use of software only, being easy and less expensive, however, such an approach is slowest among all [5-10]. Many ways exist to increase the speed of the fuzzy systems and the prominent is to use fuzzy processors. Fuzzy processors are faster and possess a best tradeoff between the speed and power consumption.

This paper presents the review of the hardware implementations of fuzzy processors and controllers. The first hardware realization of a fuzzy logic processor was done by Togai and Watanabe [11-12]. They proposed a dynamically re-configurable and cascadable architecture for a fuzzy processor with improved performance. Sasaki *et al.* [13] proposed a a fuzzy processor using SIMD. An efficient, bit scalable architecture of fuzzy logic processors is proposed by R. d' Amore [14]. Asim M. Murshid has designed and simulated a triangular memberships based fuzzy processor [15-21], a trapezoid memberships based fuzzy processor and multi membership based fuzzy processors. F. Sanchez and J. E. A. Cobo [22] has done the modelling and field programmable gate array implementation of fuzzy processors. E. F. Martinez [23] has designed and simulated a *rule-driven* based fuzzy processor. M. Hamzeh *et al.* [24] has developed a LEACH algorithm based power efficient fuzzy processor. A novel Ant Colony based architecture has been designed and developed by C. W. Tao *et al.* [25] .

This paper is divided into five sections. After introduction, section III describes novel fuzzy processors. The section IV describes various fuzzification methods. The section V discusses the defuzzification methods. The inference engine is being discussed in section VI. Section VII concludes the paper.

II. NOVEL FUZZY PROCESSORS

A lot of work has been done in the design and development fuzzy processors. The researchers tried to address the problems of area, power consumption and the delay associated with various fuzzy processors. Asim M. Murshid [15-21] has done a wonderful work in this field by designing, simulating and implanting some novel fuzzy logic processors. A Max-Min calculator along with a triangular membership function based fuzzy inference processor has been designed and developed by Asim M. Murhid [15-17], as shown in Fig. 1. The proposed architecture has been implemented on an FPGA. It has been observed that the proposed one power and

area efficient in comparison to the trapezoid membership function based fuzzy processor. A Gaussian membership based fuzzy inference processor has been designed and simulated by Asim M. Murhid [15-21], as shown in Fig. 2. The matching degree between the two Gaussian membership functions has been computed by proposing a novel MAX-MIN calculator. The proposed architectures are area, power and speed efficient in comparison to the existing state of the art processors, as they have reduced numbers of various arithmetic operations.

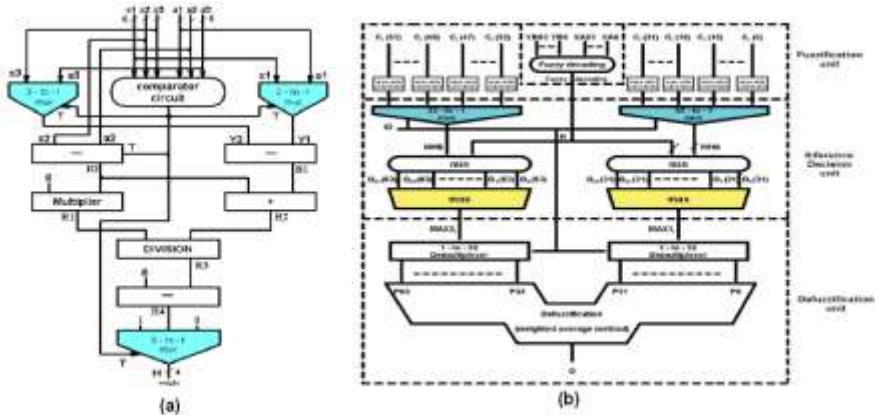

Fig. 1: (a) Triangular MF based MAX-MIN calculator (b) Proposed fuzzy inference processor [17-18].

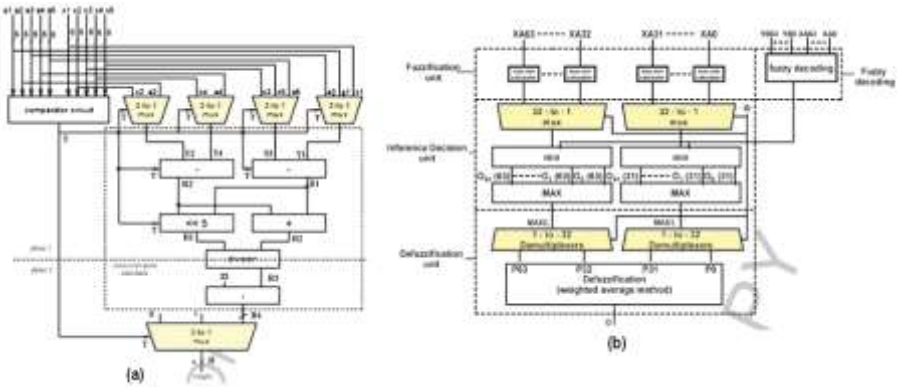

Fig. 2: (a) Trapezoid MF based MAX-MIN calculator (b) Proposed fuzzy inference processor [17-20].

Asim M. Murshid [16] has proposed a novel multi membership function based fuzzy inference processor. The processor is based on a novel architecture of a MAX-MIN calculator used for calculating the MD between the fuzzified input and the antecedent MFs. The novelty of a MAX-MIN calculator lies in calculating the MD between not only one type of MFs, but between Gaussian, Trapezoid and triangular MFs together. It is a multi membership function (MMF) MAX-MIN calculator. This is the first time that a MAX-MIN calculator with such flexibility has been designed and implemented. The proposed MMF based MUX-MIN circuit consumes reduced hardware in comparison to the fuzzy processors employing these membership functions seperatively. A significant reduction in power, pace and area has been observed in the proposed circuitry.

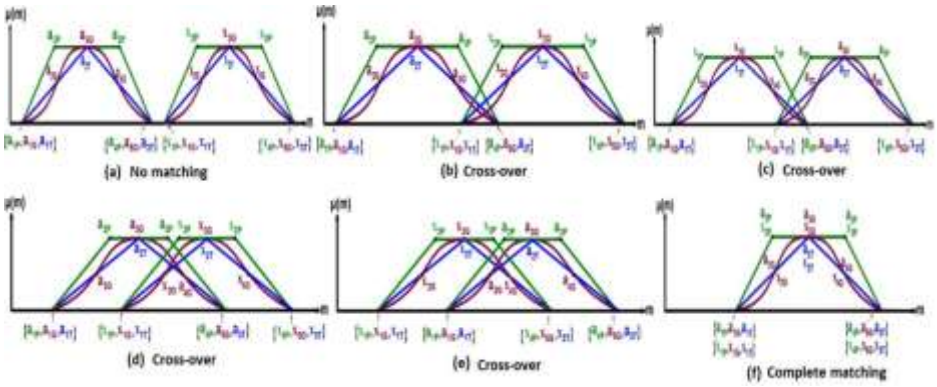

Fig. 3. Various MMFs for MAX-MIN calculation [16-18].

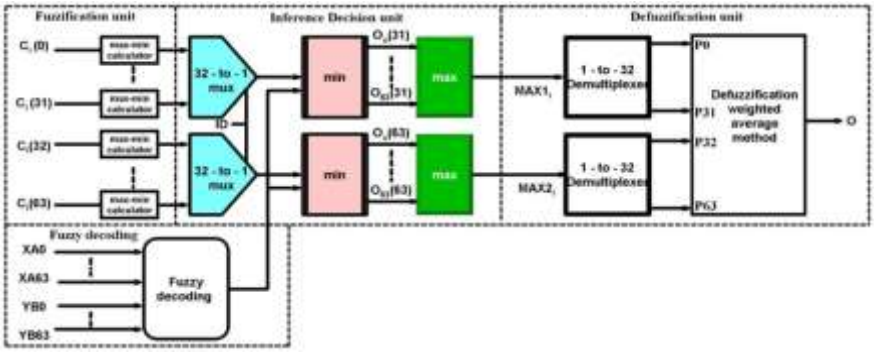

Fig. 4. Complete fuzzy processor architecture [16-18]..

III. FUZZIFIER CIRCUITS USED IN FUZZY PROCESSORS

An important operation performed by a fuzzy processor is Fuzzification. A fuzzifier converts a crisp value into a fuzzy value and actually incorporates a fuzziness, uncertainty, vagueness or ambiguity in the crisp quantity. A lot of work has been done to improve the performance of the fuzzifier in fuzzy processor. A novel fuzzifier has been designed by Hamed *et al.* [26] in an analog CMOS fuzzy logic controller. This fuzzifier generates stable, ac-curate and precise membership functions, as shown in Fig. 5(a). A. Gabrielli *et al.* [27] have designed a 4 input high speed fuzzy processor, with a novel fuzzifier block. The fuzzifier possesses four memories which store four points of a trapezoidal membership function, as shown in Fig. 5(b).

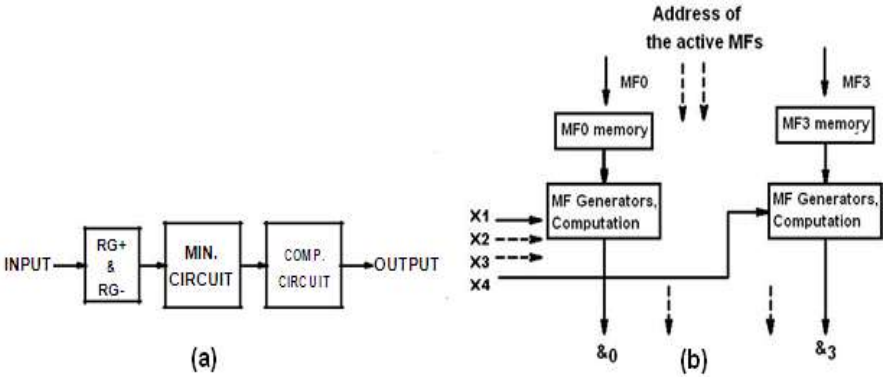

Fig. 5: (a) Fuzzifier [26] (b) Fuzzifier [27]

P. M. E. Gomes *et al.* [15] proposed a novel bit scalable architecture for fuzzy processors, employing a flexible fuzzification unit. The fuzzifier uses two comparators and the number of clock cycles does not increase drastically. A pulse width-modulation (PDM) fuzzifier is being designed and simulated by P. Ansgar *et al.* [15], as shown in Fig. 6(a). M. Y. Hassan and W. F. Sharif [28] designed a PID fuzzy controller. The Fuzzification is being done is by two blocks, for each input variable. The fuzzifier constitutes three modules, memory, inverter and incrementer, as shown in Fig. 6(b). M. Jacomet and R. Walti [29] and C. F. Juang and J. S. Chen [30] too have designed high performance fuzzifiers.

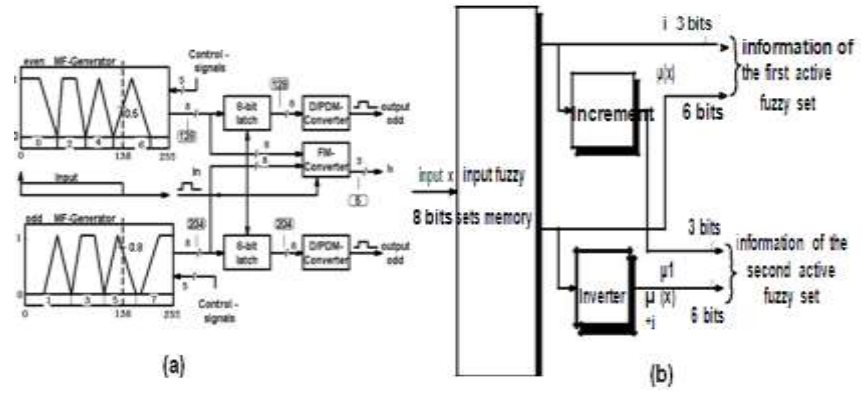

Figure 6. (a) Fuzzifier for PDM-signals [28] and fuzzifier for PID controller [15, 29].

IV. DESIGN OF DE-FUZZIFIER CIRCUITS USED IN FUZZY PROCESSORS

The conversion of fuzzy data into crisp one is defuzzification. This is an important part of fuzzy processors as the fuzzy data directly is not suitable for the real time applications. The various defuzzification methods include (a) Max-membership principle (b) Centroid method. (c) Weighted average method (c) Mean-max membership (d) Centre of sums (E) Center of largest area. These methods have their own advantages, limitations and applications. The various defuzzifiers designed are discussed in this section. J. M. Jou *et al.* [35] designed a fuzzy logic controller. The defuzzifier designed by them is based on the center of gravity method, as shown in Fig. 7(a). R. d'Amore *et al.* [14] designed bit scalable architecture for fuzzy processors. The de-fuzzifier designed is unique and determining the output value according to a set of conclusions from evaluating knowledge, as shown in Fig. 7(b).

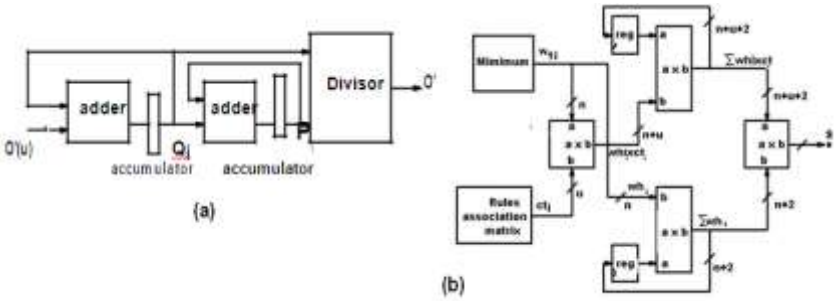

Fig. 7. (a) De-Fuzzifier [31] and Defuzzifier of [14].

The defuzzifier designed in the rule driven fuzzy processor by G. Ascia *et al.* [32] is shown in Fig. 8(a). The defuzzification is done in cooperation with the buffer circuit. A mixed signal A/D fuzzy logic controller with continuous amplitude has been designed by S. Bouras *et al.* [33]. The defuzzifier designed in this fuzzy processor is implemented using a multiplexer, a divider and three integrators, as shown in Fig. 8(b). G. Ascia *et al.* [32] have designed fuzzy processor dealing with complex fuzzy inference systems. An efficient defuzzifier has been designed as shown in Fig. 9(a), as given by Yager [34], as shown in Fig. 9(a). H. Peyravi *et al.* [26] have designed an analog fuzzy logic controller chip and implemented it in a 1.2 µm CMOS technology, as shown in Fig. 9(b). A novel defuzzifier has been designed in the proposed architecture using the center of the area method without employing a division circuit.

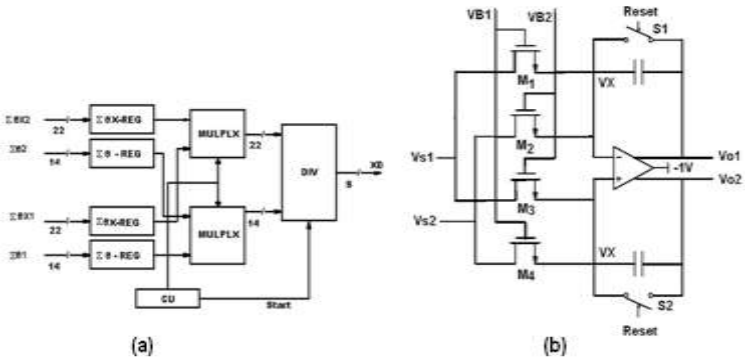

Fig. 8. (a) Block diagrams of (a) De-Fuzzifier [32] and (b) Defuzzifier of [33]

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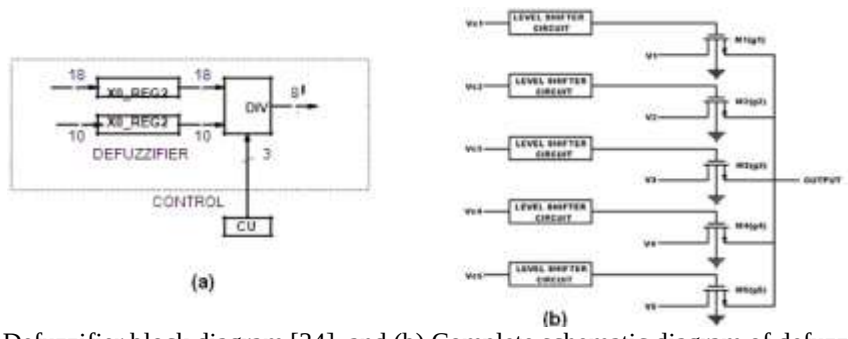

Fig. 9. (a) Defuzzifier block diagram [34] and (b) Complete schematic diagram of defuzzifier [26].

V. DESIGN OF FUZZY INFERENCE ENGINE

The fuzzy inference in a fuzzy processor means matching facts with rules, firing of the matched rules and deriving some new results. It is also being called as rule base system, expert system and fuzzy associative memory. It uses "*if*" . . ."*then*". . . statements and the connectors like "*OR* " or "*AND*" to make the required decision rule. The two well known fuzzy inference methods are Mamdani's and Sugeno methods. The Mamdani's fuzzy inference system uses fuzzy sets as a rule consequent where as the Sugeno system employs linear function of input variables as a consequent [1-4]. Various researchers have developed a lot of fuzzy inference engines with some unique properties and applications. A reconfigurable inference engine for fuzzy processors has been developed by S. Guo *et al.* [35]. The proposed engine employs Mamdani inference technique, as shown in Fig. 10(a). J. M. Jou *et al.* [36] has developed a novel inference processor for an adaptive fuzzy logic controller is shown in Fig. 10(b).

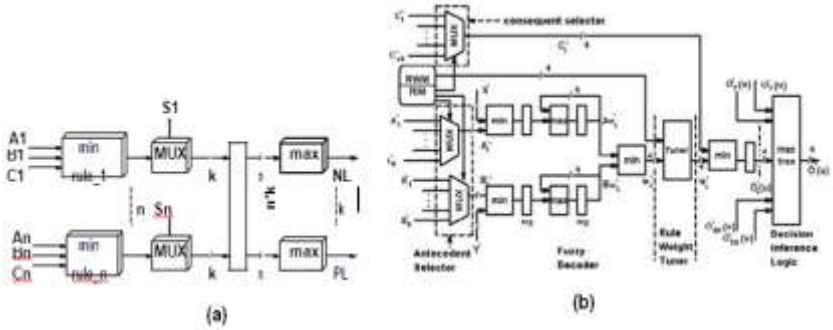

Fig. 10. (a) A reconfigurable fuzzy inference engine [35] (b) The inference engine for one rule *i* [36].

The inference engine designed and developed for a bit scalable fuzzy architecture was developed by R. d'Amore [14], as shown in Fig. 11(a). The fuzzy inference engine is based on Mamdani approach. The proposed architecture is compact and power efficient. Fig. 11(b) shows the inference engine developed by N. E. Evmorfopoulos and J. N. Avaritsiotis [37] for an adaptive digital fuzzy processor is the Sugeno model. M. Jacomet and R. Walti's [48] designed a parallel architecture for the inference machine. The proposed architecture can easily use the center of area defuzzification method. K. Nakamura *et al.* [38] have designed a fuzzy inference engine, as shown in Fig. 12. It consists of antecedents, consequents and a conventional microprocessor.

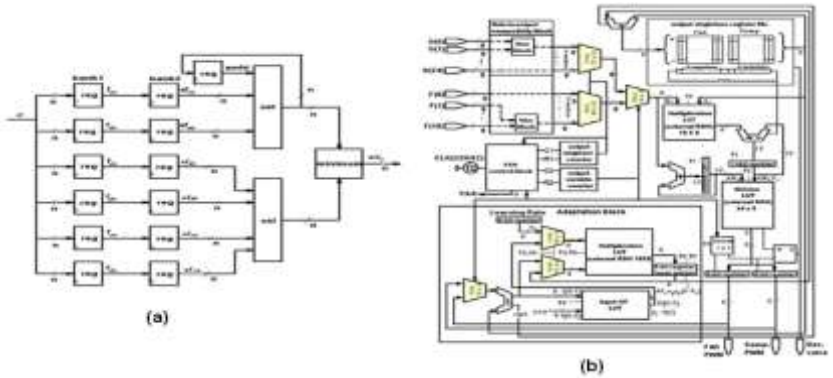

Fig. 11. (a) Inference engines [14] (b) Inference engine architecture [15].

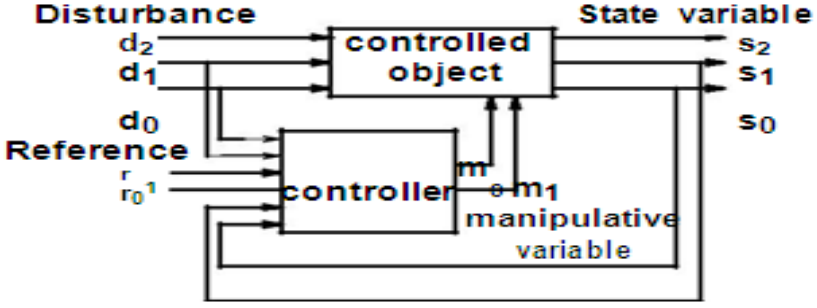

Fig. 12. Fuzzy inference control system [38].

VI. CONCLUSIONS

In this work, we presented a review of hardware implementation of fuzzy processors and controllers. Various blocks used in a fuzzy processor are discussed thoroughly. The design approaches followed to design fuzzifiers, defuzzifiers, inference engines and full blown fuzzy processors have been discussed. It has been found that a lot of work has been done to improve the performance of fuzzy processors in general and fuzzy inference engine in particular. Asim. M. Murshid has designed some unique fuzzy processors. It is the first time that a multi membership function based fuzzy processor has been designed and developed. The review has shown that there is a scope for further improvement in these fuzzy systems and their performance can be improved further by designing optimized architectures

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