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A Novel VLSI Architecture for FFT Utilizing Proposed 4:2 & 7:2 Compressor

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Abstract:- With the appearance of new innovation in the fields of VLSI and correspondence, there is likewise a perpetually developing interest for fast transforming and low range outline. It is likewise a remarkable certainty that the multiplier unit structures a fundamental piece of processor configuration. Because of this respect, rapid multiplier architectures turn into the need of the day. In this paper, we acquaint a novel structural engineering with perform high velocity duplication utilizing old Vedic math's strategies. Another fast approach using 4:2 compressors and novel 7:2 compressors for expansion has additionally been joined in the same and has been investigated. Upon examination, the compressor based multiplier present in this paper, is just about two times quicker than the mainstream routines for augmentation. Likewise we outline a FFT utilizing compressor based multiplier. This all configuration and examinations were done on a Xilinx Spartan 3e arrangement of FPGA and the timing and zone of the outline, on the same have been ascertained.

Keywords:- Fast Fourier Transform (FFT), 4:2 Compressor, Modified 4:2 Compressor, 7:2 Compressor.

I. INTRODUCTION

Advanced sign transforming (DSP) is the scientific control of a data sign to change or enhance it somehow. It is described by the representation of discrete time, discrete recurrence, or other discrete area motions by a succession of numbers or images and the transforming of these signs [1].

The objective of DSP is for the most part to gauge, channel and/or pack nonstop certifiable simple signs. The principal step is ordinarily to change over the sign from a simple to an advanced structure, by inspecting and after that digitizing it utilizing a simple to-computerized converter (ADC), which transforms the simple sign into a surge of numbers. Be that as it may, regularly, the obliged yield sign is an alternate simple yield signal, which obliges a computerized to-simple converter (DAC). Regardless of the possibility that this methodology is more unpredictable than simple handling and has a discrete worth range, the utilization of computational energy to advanced sign preparing takes into account numerous points of interest over simple transforming in numerous applications, for example, slip recognition and amendment in transmission and also information pressure. DSP calculations have long been run on standard PCs, and in addition on specific processors called advanced sign processor and deliberately manufactured equipment, for example, application-particular incorporated circuit (ASICs). Today there are extra advancements utilized for computerized sign handling including all the more capable broadly useful chip, field-programmable door clusters (FPGAs), advanced sign controllers (basically for modern applications, for example, engine control), and stream processors, among others [2-3]. The FFT is a standout amongst the most generally utilized computerized sign handling calculation. As of late, FFT processor has been broadly utilized as a part of computerized sign handling field sought OFDM, MIMO-OFDM correspondence frameworks. FFT/IFFT processors are key parts for an orthogonal recurrence division multiplexing (OFDM) based remote IEEE 802.16 broadband correspondence framework; it is a standout amongst the most complex and escalated processing module of different remote guidelines physical layer (ofdm-802.11a, MIMO-OFDM 802.11, 802.16,802.16e) [4].

II. COMPRESSOR BASED MULTIPLIER

Vedic science is an antiquated quick figuring math system which is taken from recorded old book of intelligence. Vedic science is an antiquated Vedic math which gives the exceptional procedure of mental estimation with the assistance of straightforward tenets and standards. Swami Bharati Krishna Tirtha (1884-1960), previous Jagadguru Sankaracharya of Puri selected arrangement of 16 Sutras (axioms) and 13 Sub - Sutras (culminations) from the Atharva Veda. He created strategies and methods for opening up the standards

contained in the equations and their sub-recipes, and called it Vedic Mathematics. As indicated by him, there has been extensive writing on Mathematics in the Veda-sakhas.

Vedic science is a piece of four Vedas (books of shrewdness). It is a piece of Sthapatya- Veda (book on structural building and construction modeling), which is an upa-veda (supplement) of Atharva Veda. It covers clarification of a few present day numerical terms including number-crunching, geometry (plane, co-ordinate), trigonometry, quadratic comparisons, factorization and even analytics.

a. 4:2 Compressor

To add binary numbers with minimal carry propagation we use compressor adder instead of other adder. Compressor is a digital modern circuit which is used for high speed with minimum gates requires designing technique. This compressor becomes the essential tool for fast multiplication adding technique by keeping an eye on fast processor and lesser area.

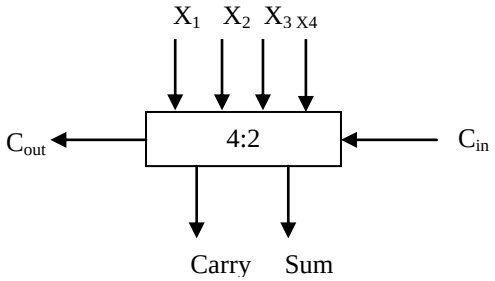
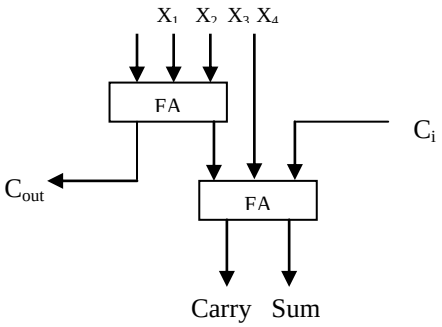


Figure 1: Block Diagram of 4:2 Compressors

4:2 compressors are capable of adding 4 bits and one carry, in turn producing a 3 bit output. The 4-2 compressor has 4 inputs X_1, X_2, X_3 and X_4 and 2 outputs Sum and Carry along with a Carry-in (Cin) and a Carry-out (Cout) as shown in Figure 1. The input Cin is the output from the previous lower significant compressor.
The Cout is the output to the compressor in the next significant stage. The critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders and half adders. Similar to the 3-2 compressor the 4-2 compressor is governed by the basic equation

$$X_1 + X_2 + X_3 + X_4 + C_{in} = Sum + 2 * (Carry + C_{out}) \quad (1)$$

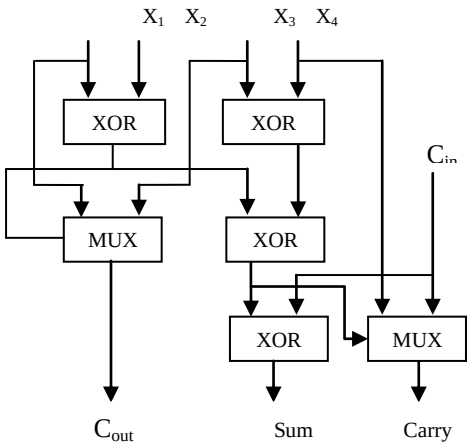


(a)

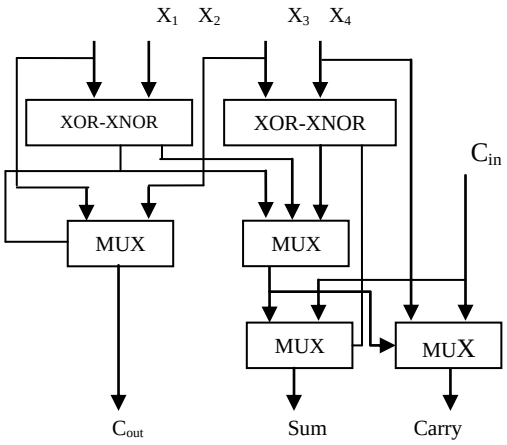
The standard implementation of the 4-2 compressor is done using 2 Full Adder cells as shown in Figure 2(a). When the individual full Adders are broken into their constituent XOR blocks, it can be observed that the overall delay is equal to 4*XOR. The block diagram in Figure 2(b) shows the existing architecture for the implementation of the 4-2 compressor with a delay of 3*XOR. The equations governing the outputs in the existing architecture are shown below

$$Sum = X_1 \oplus X_2 \oplus .X_3 \oplus X_4 \oplus C_{in} \quad (2)$$

$$Cout = (X_1 \oplus X_2).X_3 + \overline{(X_1 \oplus X_2)}.X_1 \quad (3)$$



(b)



(c)

Figure 2: Design of 4:2 compressor using (a) full adder, (b) XOR and Multiplexer, (c) Proposed 4:2 Compressor

$$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X_4) \cdot C_{in} + \overline{(X_1 \oplus X_2 \oplus X_3 \oplus X_4)} \cdot X_4 \quad (4)$$

However, like in the case of 3-2 compressor, the fact that both the output and its complement are available at every stage is neglected. Thus replacing some XOR blocks with multiplexer's results in a significant improvement in delay. Also the MUX block at the SUM output gets the select bit before the inputs arrive and thus the transistors are already switched by the time they arrive. This minimizes the delay to a considerable extent. This is shown in Figure 2(c).

The equations governing the outputs in the proposed architecture are shown below

$$Sum = (X_1 \oplus X_2).(X_3 \oplus X_1) + (X_1 \oplus X_2).C_{in} \quad (5)$$

$$Cout = (X_1 \oplus X_2).X_3 + \overline{(X_1 \oplus X_2)}.X_1 \quad (6)$$

$$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X_4) \cdot C_{in} + \overline{(X_1 \oplus X_2 \oplus X_3 \oplus X_4)} \cdot X_4 \quad (7)$$

b. 7:2 Compressor

Similar to its 4:2 compressor counterpart, the 7:2 compressor as shown in Figure 3, is capable of adding 7 bits of input and 2 carry's from the previous stages, at a time. In our implementation, we have designed

a novel 7:2 compressor utilizing two 4:2 compressors, two full adders and one half adder. The architecture for the same has been shown in Figure 4.

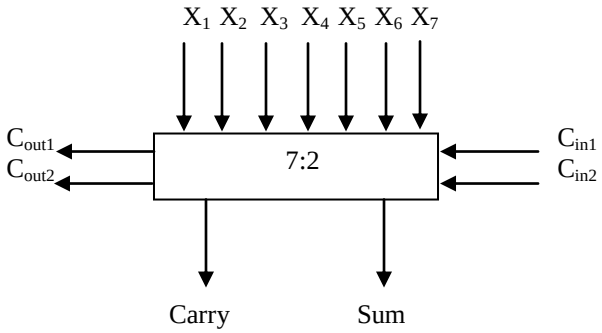


Figure 3: Block Diagram of 7:2 Compressor

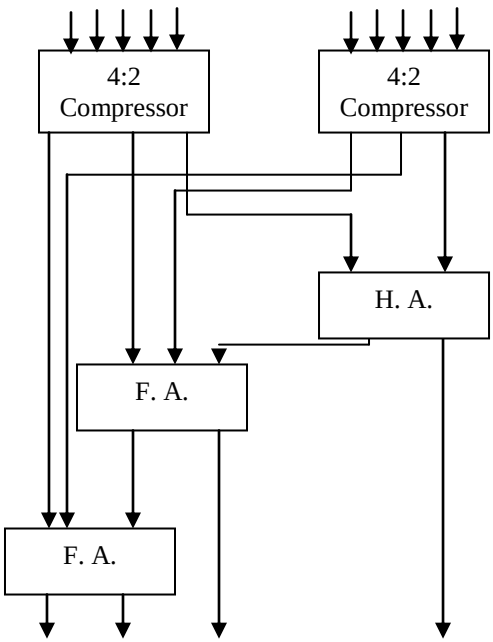


Figure 4: 7:2 Compressor using 4:2 Compressor

III. FAST FOURIER TRANSFORM

The decimation, however, causes shuffling in data. The entire process involves $v = \log_2 N$ stages of decimation, where each stage involves $N/2$ butterflies of the type shown in the Figure 5.

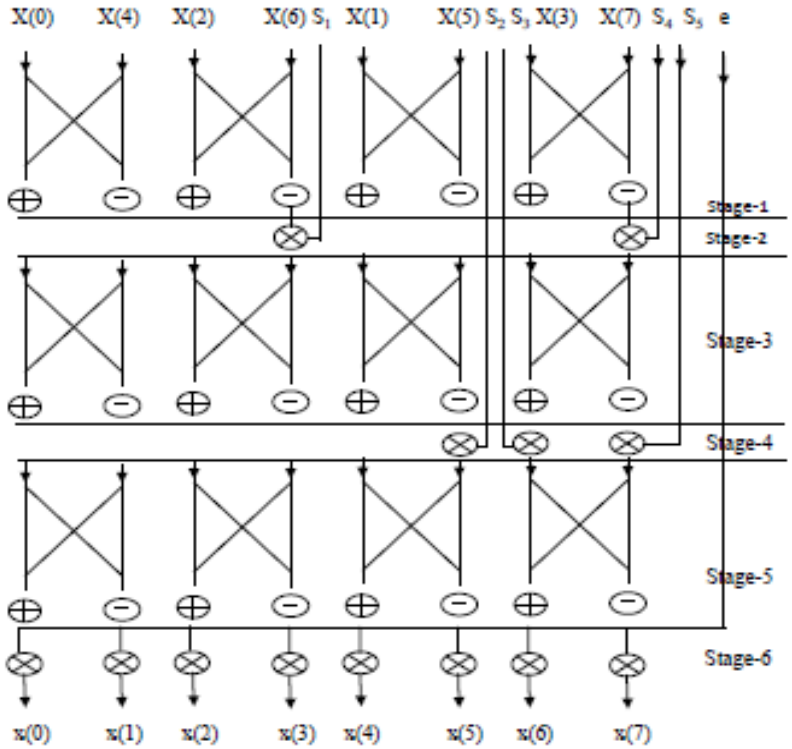


Figure 5: Block Diagram of 8-point Fast Fourier Transform

IV. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 14.1i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. By the aid of that software we debug the program easily. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Spratan-3 FPGAs. With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing. We functionally verified each unit presented in this paper including all three 4:2 Compressor, 7:2 Compressor, Compressor based Multiplier and 8-point fast fourier transform. We have been found from the results shown in Table 1 to Table 4 respectively, that number of slices used is same in case of 4:2 compressor adder and 4:2 modified compressor adder which is less than slices used in 4:2 proposed compressor adder. So we designed fast fourier transform using 4:2 & 7:2 compressor based multiplier, 4:2 & 7:2 modified compressor based multiplier and proposed 4:2 & 7:2 proposed compressor based multiplier whose device utilization summary is given in Table.

Table 1: Device utilization summary (Spartan 3) of 4:2 Compressors, Modified 4:2 Compressor and Proposed 4:2 Compressor

Design	No. of slices	No. of 4 input LUTs	MCPD (ns)
4:2 Compressor	**3**	**6**	**10.764**
Modified 4:2 Compressor	**2**	**4**	**9.344**
Proposed 4:2 Compressor	**2**	**3**	**8.138**

Table 2: Device utilization summary (Spartan 3) of 7:2 Compressors, Modified 7:2 Compressor and Proposed 7:2 Compressor

Design	No. of slices	No. of 4 input LUTs	MCPD (ns)
7:2 Compressor	9	17	13.656
Modified 7:2 Compressor	7	12	12.383
Proposed 7:2 Compressor	7	11	12.147

Table 3: Device utilization summary (Spartan 3) of Compressors based Multiplier, Modified Compressor based Multiplier and Proposed Compressor based Multiplier

Design	No. of slices	No. of 4 input LUTs	MCPD (ns)
Compressor based Multiplier	**108**	**190**	**55.050**
Modified Compressor based Multiplier	**78**	**143**	**41.684**
Proposed Compressor based Multiplier	**79**	**142**	**33.614**

Table 4: Device utilization summary (Spartan 3) of Fast Fourier Transform (FFT)

Design	No. of slices	No. of 4 input LUTs	MCPD (ns)
FFT using Compressor based Multiplier	**312**	**549**	**29.905**
FFT using Modified Compressor based Multiplier	**162**	**286**	**22.867**
FFT using Proposed Compressor based Multiplier	**128**	**227**	**21.166**

V. CONCLUSION

Quick fourier change (FFT) is utilized to change over intricate and genuine qualities into genuine and complex ones. It obliges decay of information into stages utilizing butterfly like DFT. Yet the butterfly utilized as a part of FFT is truly distinctive regarding coefficients or multipliers. With the increment in number of FFT arrangement length the quantity of coefficients is likewise expanded at the same time. Deferral gave and range needed by equipment is the two key components which are have to be consider. Here we display FFT utilizing diverse sorts of compressor based multiplier.

Among all three designs, proposed compressor based multiplier provides the least amount of Maximum combinational path delay (MCPD). Also, it takes least number of slices i.e. occupy least area among all three design.

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