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Estimation of Crosstalk Noise for 2π RC and RLC Interconnects in Deep Submicron VLSI Circuits

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Abstract:- Crosstalk noises have been estimated both for RC and RLC interconnects, respectively, in deep submicron VLSI circuits. The 2π model approach has been employed. The victim line is considered as an RC or RLC line, and the aggressor line is placed near the victim line. The aggressor line is excited with a voltage pulse at the coupling location keeping the victim line quiet. Analytical expressions of the output crosstalk noise voltages have been derived, and then the values of the peak noise voltages have been calculated. Subsequently, simulation work by HSPICE has been performed. The result shows an output crosstalk peak noise estimation of 6.29% error on average and that of 5.77% error on average compared with HSPICE simulation both for 2π RC and RLC interconnects, respectively.

Keywords:- Crosstalk noise, Interconnect, Deep submicron, 2π model, Victim line, Aggressor line, VLSI circuit.

I. INTRODUCTION

Continuous scaling of MOS transistor and the increase of circuit complexity are making the role of interconnect in deep submicron (DSM) VLSI circuits more prominent. DSM technology is the technology where transistors of smaller size with faster switching rates are used. Technologies beyond the feature sizes of 0.25 μm are usually referred as DSM technologies. Several issues, such as, signal integrity, low-power design, high-density and design complexity, packing and testing, cost-effectiveness are challenging in DSM technology, where the signal integrity issue is very much critical. The major concerning signal integrity issues are crosstalk noise, crosstalk delay and electro-migration. These issues can lead to chip failure, if these issues are not addressed rightly in right time. In DSM technology, crosstalk noise has recently become more crucial due to capacitive coupling between lines/wires as well as inductive effect [1 – 3]. The line which suffers is referred to as victim, and the neighbouring line which contributes to coupling/inductive noise on the victim is referred to as aggressor. If the crosstalk noise effects on the victim line are large, they can propagate into storage elements that connect to victim line and can cause permanent errors. Intensive researches have been going on for proposing better models for accurate estimation of crosstalk noise for RC and RLC interconnects [1-6]. Different analytical models, such as, π and L models, have been proposed taking R, L, C as lumped and/or distributed parameters in the lines/wires. Recently π-model has become more popular. Along with analytical analysis, SPICE simulation in the circuit level has drawn special attraction due to time-saving as well as justification perspective.

In this study, the 2π model approach has been employed for analytical study in time domain. The victim line is considered as an RC or RLC line. An aggressor line is placed near the victim line, as shown in Fig. 1. The aggressor line is excited with a voltage pulse, such as, a unit step input [2] for RC interconnect and the input reported by Sahoo et. el [3] for RLC interconnect at the coupling location keeping the victim line quiet. After analytical investigation, SPICE simulation in the circuit level has been performed using HSPICE software platform. The results obtained from analytical study have been compared with the results obtained by HSPICE simulation both for 2π RC and RLC interconnects, respectively. It reveals that the output of the investigation is appreciable.

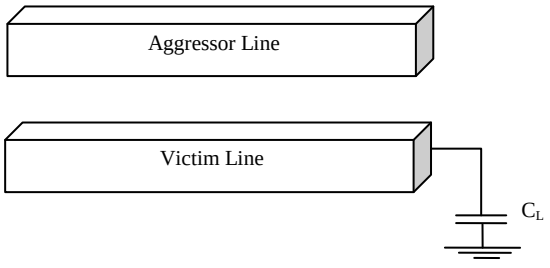


Fig. 1: Layout of aggressor and victim lines

II. MATERIALS AND METHODS

A. Derivation of Crosstalk Noise for 2 □ RC Interconnect

The equivalent circuit of Fig. 1 is shown in Fig. 2, in the form of 2π type RC model, to derive the analytical expression of crosstalk noise voltage in time domain. This model contains two π type RC circuits – one π type RC circuit is located before the coupling and the other is after the coupling. The victim driver is modelled by an effective resistance R_d and the other RC parameters are C_x, C_1, R_s, C_2, R_e and C_L, as shown in Fig. 2 which is redrawn, as shown in Fig. 3.

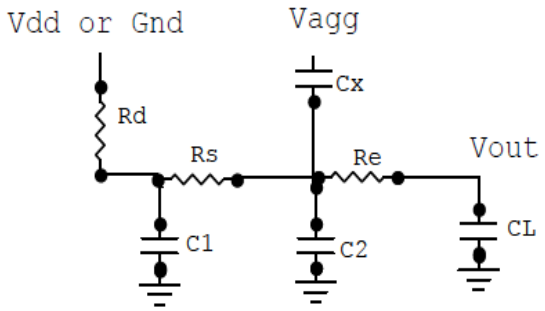


Fig. 2: Equivalent circuit of victim and aggressor lines in the form of 2 □ type RC model

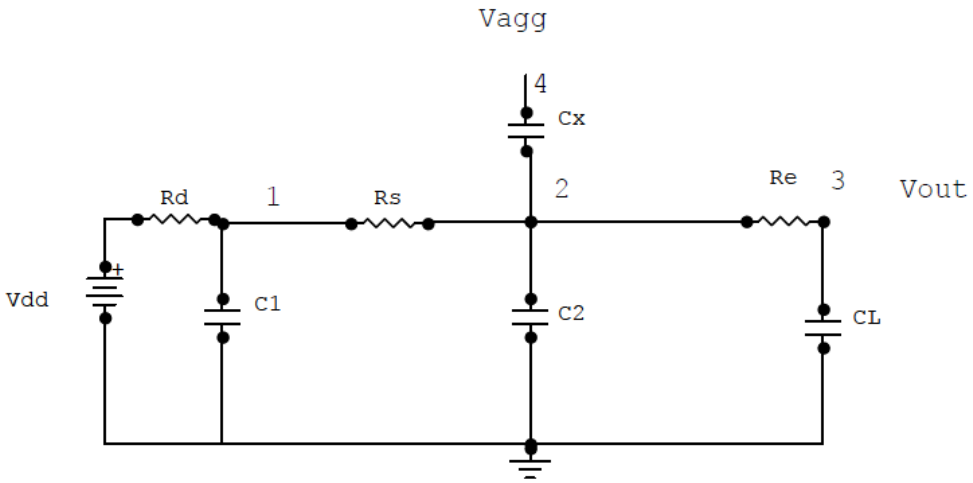


Fig. 3: Equivalent circuit of 2 □ type RC model, redrawn from Fig.2

From Fig. 3, the impedances Z_1 at node 1 and Z_2 at node 2 in s-domain are obtained as,

$$Z_1 = \frac{R_d}{1 + sR_dC_1} \tag{01}$$

$$\frac{1}{Z_2} = \frac{1}{(Z_1 + R_s)} + sC_2 + \frac{1}{\left(R_e + \frac{1}{SC_L}\right)} \tag{02}$$

Therefore, the voltage $V_2(s)$ at node 2 across the impedance Z_2 in s-domain is found as,

$$V_2(s) = \frac{Z_2}{Z_2 + \frac{1}{sC_x}} V_{agg}(s) \tag{03}$$

Finally the output voltage V_{out} in s-domain becomes,

$$V_{out}(s) = V_2(s)\frac{\frac{1}{sC_L}}{R_e + \frac{1}{sC_L}} \tag{04}$$

Manipulating the Equations (01) – (04), $V_{out}(s)$ can be represented in the form as,

$$V_{out}(s) = \frac{a_2 s^2 + a_1 s}{s^3 + b_2 s^2 + b_1 s + b_0} V_{agg}(s) \tag{05}$$

The coefficient are defined as,

$$a_1 = \frac{C_x(R_d + R_s)}{K_2},\quad a_2 = \frac{K_1}{K_2},\quad b_0 = \frac{1}{K_2},\quad b_1 = \frac{(C_x + C_2)(R_d + R_s) + (R_d C_1 + C_L R_e) + C_L(R_d + R_s)}{K_2},$$

$$\text{and}\quad b_2 = \frac{(C_x + C_2)\{R_d R_s C_1 + C_L R_e\} + \{R_d R_e C_1 C_L + R_d R_s C_1 C_L\}}{K_2}.$$

Using dominant-pole approximation method [3], the Equation (05) can be simplified in the form as,

$$V_{out}(s) = \frac{a_1 s}{b_1 s + b_o} V_{agg}(s) \tag{06}$$

Now applying unit step input with normalized $V_{dd} = 1$ in the aggressor, i.e.,

$$V_{agg}(s) = \frac{1}{s}$$

The Equation (06) becomes,

$$V_{out}(s) = \frac{a_1}{b_1 s + b_o} \tag{07}$$

Putting the values of a_1, b_1 and b_0 in Equation (07), and then manipulating, we found $V_{out}(s)$ as,

$$V_{out}(s) = \frac{t_x}{t_v(s + \frac{1}{t_v})} \tag{08}$$

Here, t_x is the RC delay term from the upstream resistance of the coupling element and the coupling capacitance. And t_v is the distributed Elmore delay [1] of victim line. Mathematically,

$$t_x = C_x(R_d + R_s),\quad \text{and}\quad t_v = (C_x + C_2)(R_d + R_s) + (R_d C_1 + C_L R_e) + C_L(R_d + R_e)$$

The output voltage shown in Equation (08) is in s-domain, and can be expressed in time domain as,

$$V_{out}(t) = \frac{t_x}{t_v} e^{-\frac{t}{t_v}},\quad \text{where}\quad t \geq 0 \tag{09}$$

The Equation (09) reveals that the output crosstalk noise voltage decreases monotonically with the condition $t \geq 0$, and the maximum value of noise is,

$$V_{\max} = \frac{t_x}{t_v} \tag{10}$$

B. Derivation of Crosstalk Noise for 2 □ RLC Interconnect

The equivalent circuit of Fig. 1 is shown in Fig. 4, in the form of 2π type RLC model, to derive the analytical expression of crosstalk noise voltage in time domain. This model contains two π type RLC circuits – one π type RLC circuit is located before the coupling and the other is after the coupling. The victim driver is modelled by an effective resistance R_d and the other RLC parameters are C_x, C_1, R_s, L_s, C_2, R_e, L_e and C_L, as shown in Fig. 4 which is redrawn, as shown in Fig. 5.

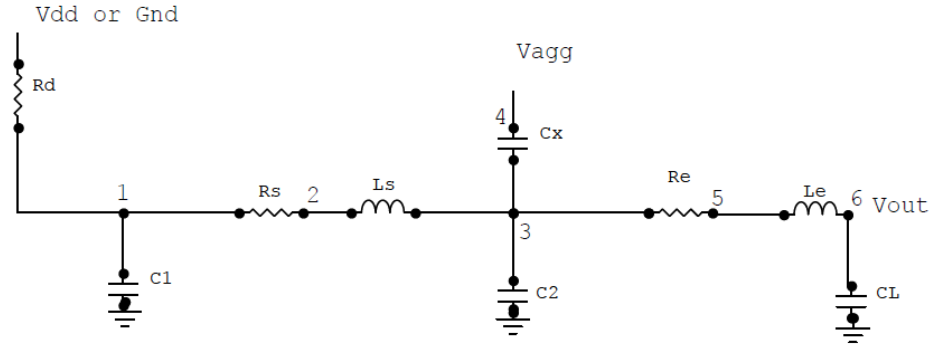


Fig. 4: Equivalent circuit of victim and aggressor lines in the form of 2 □ type RLC model

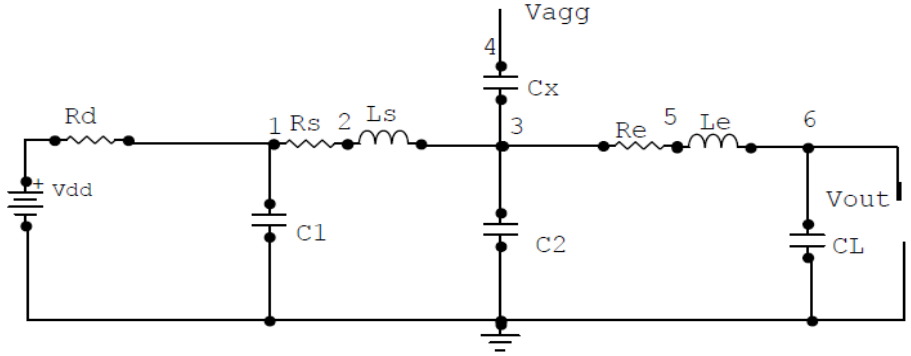


Fig. 5: Equivalent circuit of 2 □ type RLC model, redrawn from Fig. 4

From Fig. 5, the impedances Z_1 at node 1 and Z_2 at node 3 in s-domain are obtained as,

$$Z_1 = \frac{R_d}{1 + sR_dC_1} \tag{11}$$

$$\frac{1}{Z_2} = \frac{1}{(Z_1 + R_s + sL_s)} + sC_2 + \frac{1}{\left(R_e + sL_e + \frac{1}{sC_L}\right)} \tag{12}$$

Therefore, the voltage $V_2(s)$ at node 3 across the impedance Z_2 in s-domain is found as,

$$V_2(s) = \frac{Z_2}{Z_2 + \frac{1}{sC_x}} V_{agg}(s) \tag{13}$$

Finally the output voltage V_{out} in s-domain becomes,

$$V_{out}(s) = V_2(s) \frac{1}{sC_LR_e + s^2L_eC_L + 1} \tag{14}$$

Manipulating the Equations (11) – (14), $V_{out}(s)$ can be represented in the form as,

$$V_{out}(s) = \frac{a_3 s^3 + a_2 s^2 + a_1 s}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} \times V_{agg}(s) \tag{15}$$

The coefficient are defined as,

$$a_3 = C_x R_d L_s C_1, a_2 = (R_d R_s C_1 + L_s), a_1 = C_x (R_d + R_s)$$

$$b_5 = (C_x + C_2)(R_d + R_s) L_e C_L, b_4 = (C_x + C_2)(R_d R_s C_1 L_e C_L + R_d L_s C_1 R_e C_L)$$

$$b_3 = (C_x + C_2)\{(R_d + R_s) L_e C_L + L_s L_e C_L + R_d R_s C_1 R_e C_L + R_e L_s C_L + R_d L_s C_1\} + R_d C_1 L_e C_L + R_d L_s C_1 C_L$$

$$b_2 = (C_x + C_2)\{(R_d + R_s) R_e C_L + L_s + R_d R_s C_1 + L_e C_L + R_d C_1 R_e C_L + C_L (L_s + R_d R_s C_1)\}$$

$$b_1 = (C_x + C_2)(R_d + R_s) + R_e C_L + R_d C_1 + C_L (R_d + R_s)$$

Using dominant-pole approximation method [3], the Equation (15) can be simplified in the form as,

$$V_{out}(s) = \frac{C_x s(a_1 s + a_0)}{p_2 s^2 + p_1 s + 1} V_{agg}(s) \tag{16}$$

where,

$$p_2 = \left[C_L L_e + (C_x a_0 + b_1) R_e C_L + (C_x a_1 + b_2)\right], \quad p_1 = \left[(C_x a_0 + b_1) + R_e C_L\right] \text{ and } \quad a_0 = (R_s + R_d)$$

Now applying the input as reported by Sahoo et. el [3] in the aggressor, i.e.,

$$V_{agg}(s) = \left[\frac{\frac{1}{t_r}}{s\left[\left(\frac{a_2}{t_r} + a_1\right)s^2 + \left(\frac{a_1}{t_r} - 1\right)s + \frac{1}{t_r}\right]} \right]$$

The Equation (16) becomes,

$$V_{out}(s) = \left(\frac{C_x s(a_1 s + a_0)}{p_2 s^2 + p_1 s + 1} \right) \times \left[\frac{\frac{1}{t_r}}{s\left[\left(\frac{a_2}{t_r} + a_1\right)s^2 + \left(\frac{a_1}{t_r} - 1\right)s + \frac{1}{t_r}\right]} \right] \tag{17}$$

Again using dominant-pole approximation method [3], the Equation (17) can be simplified in the form as,

$$V_{out}(s) = \frac{A_8}{s + \alpha_3} + \frac{A_9}{s + \beta_3} \tag{18}$$

where,

$$A_8 = \frac{\frac{C_x}{t_r}(a_0 - a_1 \alpha_3)}{\beta_3 - \alpha_3} \text{ and } A_9 = \frac{\frac{C_x}{t_r}(a_0 - a_1 \beta_3)}{\alpha_3 - \beta_3}$$

$$\alpha_3, \beta_3 = -\frac{\left(\frac{p_1}{t_r} + \frac{a_1}{t_r} + 1\right)}{2} \pm \sqrt{\left(\frac{\left(\frac{p_1}{t_r} + \frac{a_1}{t_r} + 1\right)^2}{4} - \left[\left(\frac{a_2}{t_r} + a_1\right) + \left(\frac{a_1}{t_r} + 1\right)p_1 + \frac{p_2}{t_r}\right]\frac{1}{t_r} \right)}.$$

The output voltage shown in Equation (18) is in s-domain, and can be expressed in time domain as,

$$V_{out}(t) = A_8 e^{-\alpha_3 t} + A_9 e^{-\beta_3 t} \tag{19}$$

The Equation (19) reveals that the output crosstalk noise voltage decreases exponentially as honey-comb of two factors, and the peak value of noise can be found as,

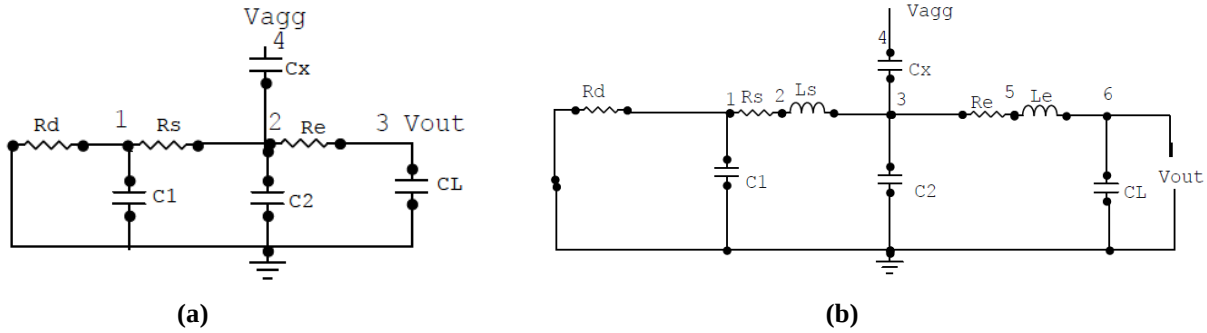
$$V_{peak} = A_8 e^{-\alpha_3 t_{peak}} + A_9 e^{-\beta_3 t_{peak}} \tag{20}$$

where,

$$t_{peak} = \frac{1}{\alpha_3 - \beta_3} \ln\left[\frac{\alpha_3(a_0 - a_1\alpha_3)}{\beta_3(a_0 - a_1\beta_3)}\right]$$

C. HSPICE Simulation

We use HSPICE for circuit simulation and the circuits for simulation are shown in Figs. 6(a) and (b) for RC and RLC interconnects, respectively. The maximum output crosstalk noise voltage expressions are found in Equations (10) and (20) for RC and RLC interconnects, respectively.



(a) **(b)**

Fig. 6: Equivalent circuit for simulation by HSPICE: (a) for RC interconnect and (b) for RLC interconnect

III. RESULTS AND DISCUSSION

We simulated the output noise voltage by using HSPICE and compared the simulated results with the analytical results observed in 2π RC and 2π RLC models.

A. Noise Estimation for 2π RC Interconnect

Unit step input is used in aggressor line keeping victim line as quiet for noise estimation in 2π RC interconnect. Fig. 6(a) is used for simulation by HSPICE. Fig. 7 shows the output noise voltage in time domain across victim capacitor (C_L) at node 3 of Fig. 6(a) for 2π RC interconnect. From constant 40 ms the voltage is increasing so fast and then after saturation label at 80 ms again the voltage is decreasing directly and goes to below zero (0) label and then goes to directly constant voltage upto 160 ms and then again at this time the voltage is growing up above zero (0) label and then will be constant with respect to increasing time.

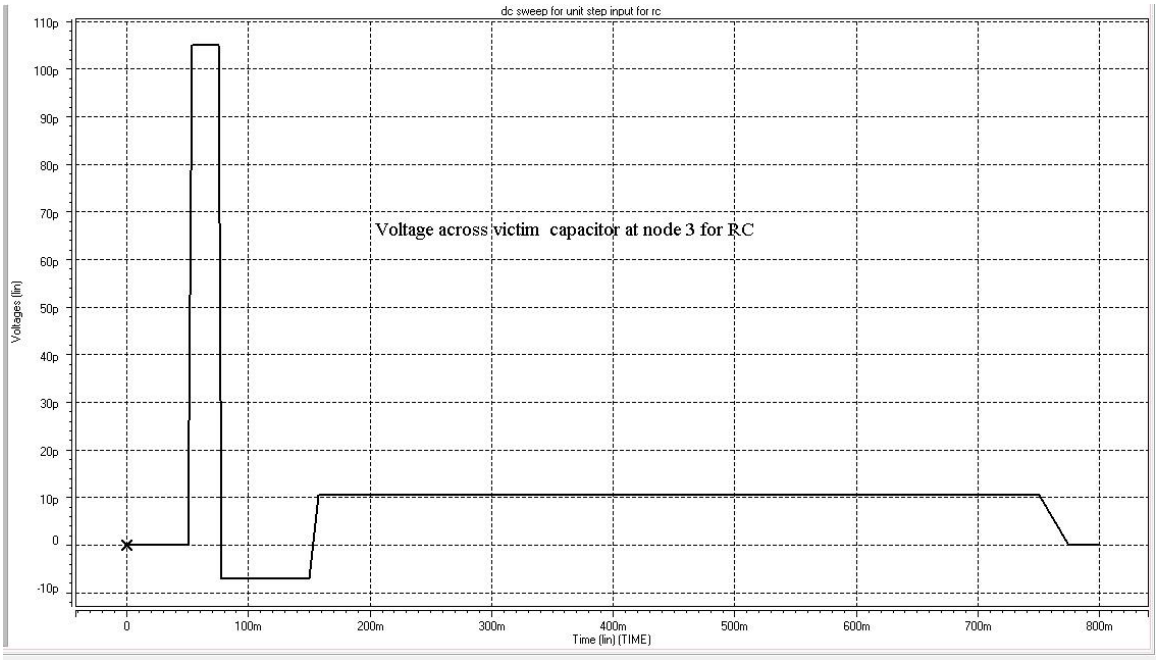


Fig. 7: Output noise voltage in time domain across victim capacitor C_L at node 3 of Fig. 6(a) for 2π RC interconnect, where R_d = 50 Ω, R_e = 20 Ω, R_s = 20 Ω, C_x = 150 fF, C_L=10 fF

Fig. 8 shows the voltage across victim capacitor C_L at node 3 of Fig. 6(a) with respect to frequency. The figure shows that voltage is approximately increasing with respect to increasing frequency.

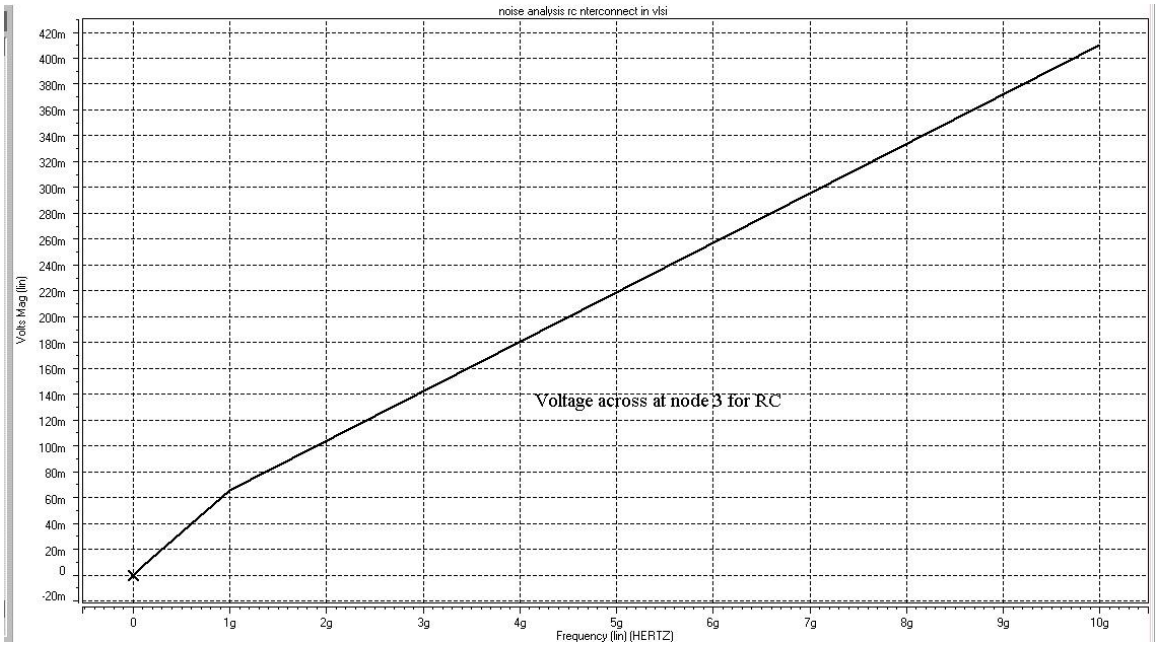


Fig. 8: Voltage in frequency domain across victim capacitor C_L at node 3 of Fig. 6(a) for 2π RC interconnect, where R_d = 50 Ω, R_e = 20 Ω, R_s = 20 Ω, C_x = 150 fF, C_L=10fF

We perform the simulation program by HSPICE. Fig. 9 shows the output crosstalk noise voltage waveforms in frequency domain of RC interconnect in DSM VLSI circuit for unit step aggressor input. While performing simulation by HSPICE, we use the maximum frequency of 10 GHz. When the frequency is increasing, the noise voltage is decreasing gradually, as seen in the Fig. 9.

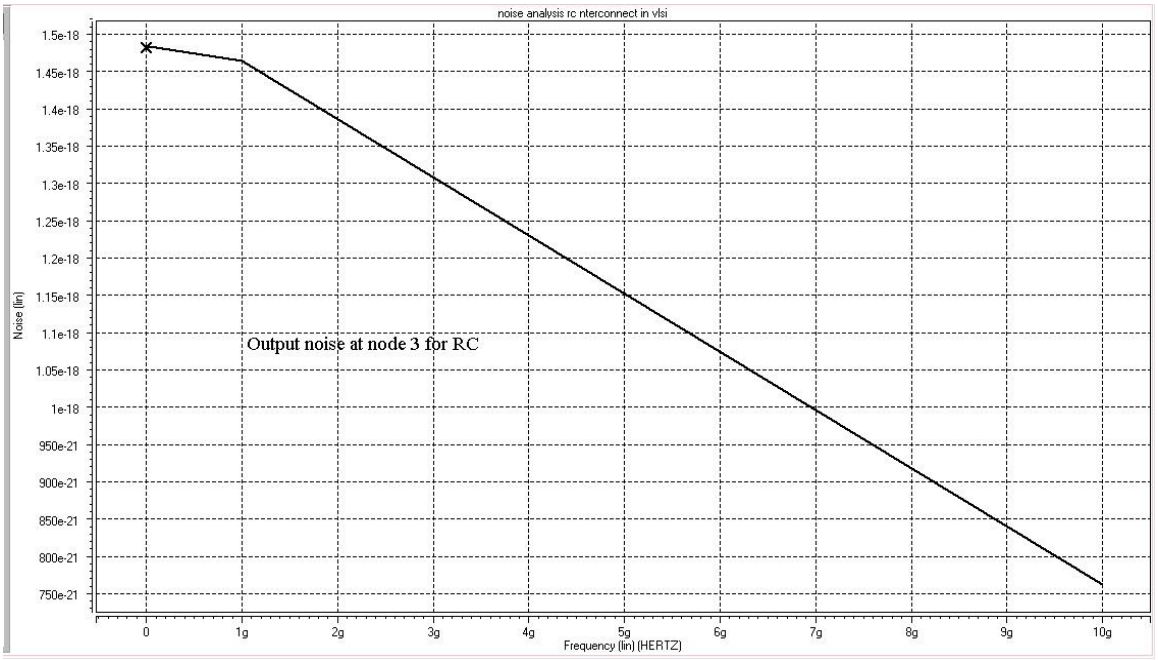


Fig. 9: Output crosstalk noise voltage waveform in frequency domain by HSPICE simulation for RC interconnect, where R_d = 50 Ω, R_e = 20 Ω, R_s = 20 Ω, C_1 = 50 fF, C_2 = 100 fF, C_x = 150 fF and C_L = 10 fF

After simulation work, we calculated the peak values of the output crosstalk noise voltage using the Equation (10). The peak values of the output crosstalk noise voltage for both the calculated and simulated data are summarized in Table I. And then we compared the simulated data with the calculated data which are shown as % of error and % of average error in Table I. The table shows that the average % of error is 6.29%, which is good enough compared to the other results published in the literature [1], [2], [4], [5], [7-9]. The comparison is shown in Table II.

Table I: Comparison of Output Crosstalk Noise Peak Voltage for RC Interconnect

Sl. No.	R_d (Ω)	R_s (Ω)	R_e (Ω)	C_1 (fF)	C_x (fF)	C_2 (fF)	C_L (fF)	V_{peak} (v) (HSPICE)	V_{peak} (v) Calculated	Error (%)	Average Error (%)
1	50	20	20	50	150	100	10	0.4101058	0.50	17.97	6.29
2	100	50	50	50	150	100	15	0.4880701	0.49	0.39	
3	150	70	70	50	150	100	20	0.4936848	0.48	2.16	
4	200	100	100	50	150	100	25	0.4907008	0.47	3.60	
5	250	120	120	50	150	100	30	0.4797421	0.45	7.33	

Table II: Comparison of Average % of Error for RC Interconnect with Published Literature

	Our Work	Ref. [1]	Ref. [2]	Ref. [4]	Ref. [5]	Ref. [7]	Ref. [8]	Ref. [9]
Average Error (%)	6.29	6	2.2	5	14	4.4	8.4	13

We investigated on a RC network to compare Devgan [10], Heydari [8] and 2π analytical models with circuit simulation. Fig. 10 shows the maximum crosstalk noise voltage of RC transmission lines for unit step input. The figure shows the changes in maximum crosstalk noise voltage when the input rise time varies from 10 ps to 200 ps when all of the geometric parameters are kept constant. As seen in the figure, the 2π model is compared with Devgan named as DEV, Heydari named as HEY and circuit simulation. The figure indicates that the plot for 2π model is converging with the plot for circuit simulation for a wide range of input rise times. For long rise times, Devgan's metric predicts accurately the peak amplitude of noise. Heydari's metric is best suited for lengthy interconnects.

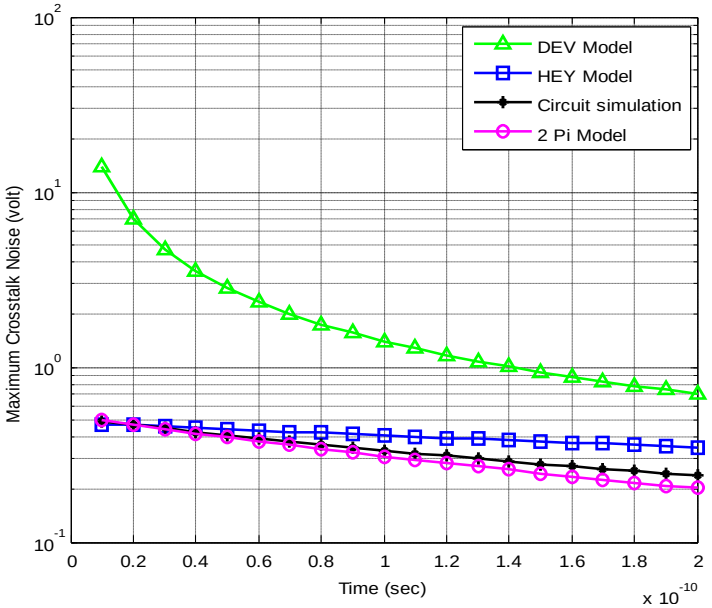


Fig. 10: Comparison of Maximum Crosstalk Noise Voltage of 2π RC Interconnect for unit step input

Fig. 11 shows the scatter diagrams which compare the Devgan, Heydari and 2π models with circuit simulations. As seen in the figure, the estimation accuracy of the Devgan model compared with the circuit simulation is not high. The estimation accuracy of the Heydari model is higher than that of the Devgan model. And the 2π model gives very good estimation, i.e., the diagram shows that the estimation accuracy of 2π model is higher than that of the other models, compared with circuit simulation.

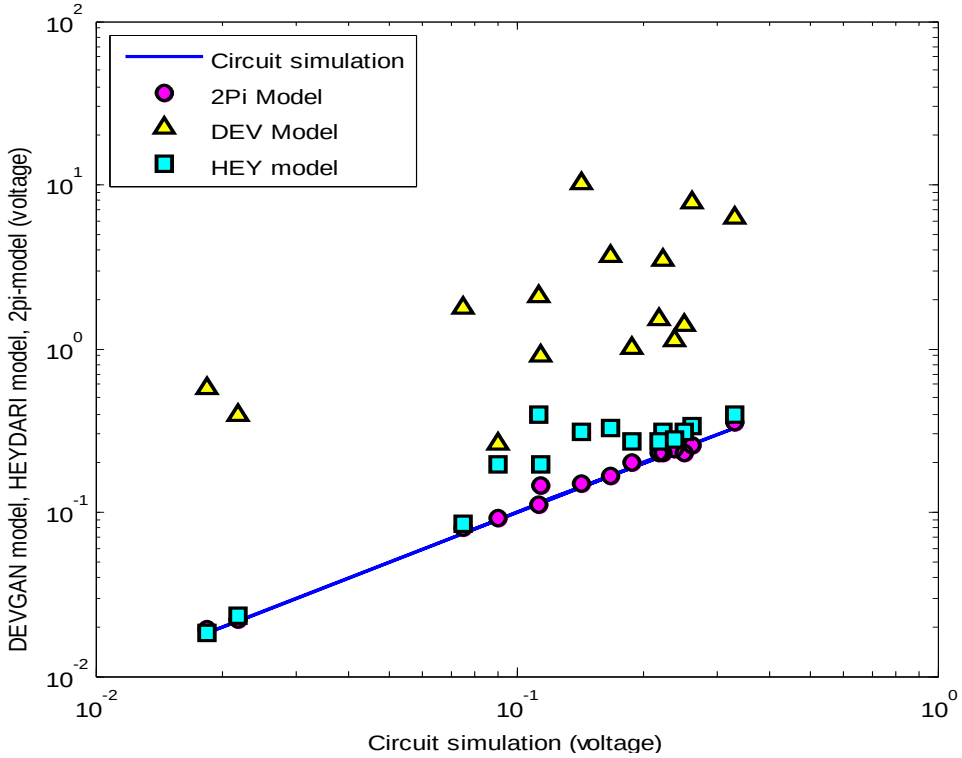


Fig. 11: Devgan/Heydari/2π model versus circuit simulation for RC interconnect for peak noise voltage for unit step input

B. Noise Estimation for 2π RLC Interconnect

The Input reported by Sahoo et. el [3] and imported for Equation (17) is used in aggressor line keeping victim line as quit for noise estimation in 2π RLC interconnect. Fig. 6(b) is used for simulation by HSPICE. Fig. 12 shows the output noise voltage in time domain across victim capacitor (C_L) at node 6 of Fig. 6(b) for 2π RLC interconnect. From constant 100 ms the voltage is increasing so fast and then after saturation label at 160 ms again the voltage is decreasing directly and at this time the voltage will be constant with respect to increasing time.

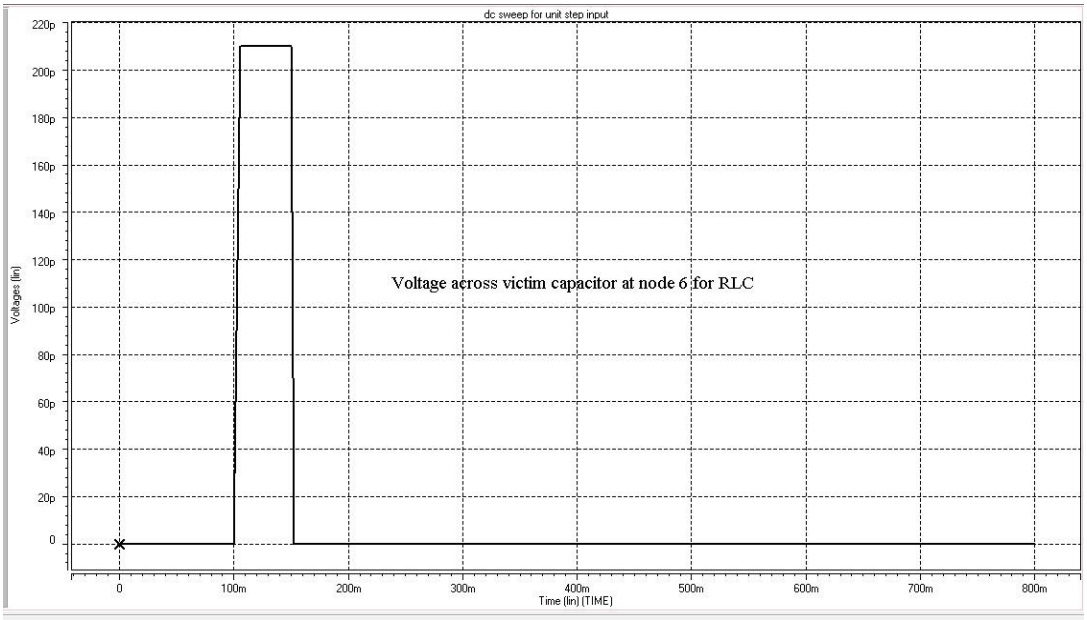


Fig. 12: Output noise voltage in time domain across victim capacitor C_L at node 6 of Fig. 6(b) for 2π RLC interconnect, where R_d = 50 Ω, $R_s = R_{1a}$ = 20 Ω, $R_e = R_{1v}$ = 20 Ω, L_s = 302 nH, L_e = 302 nH, C_1 = 50 fF, C_2 = 100 fF, C_x = 150 fF and C_L = 10 fF

Fig. 13 shows the voltage across victim capacitor C_L at node 6 of Fig. 6(b) with respect to frequency. The figure shows that voltage is approximately increasing with respect to increasing frequency.

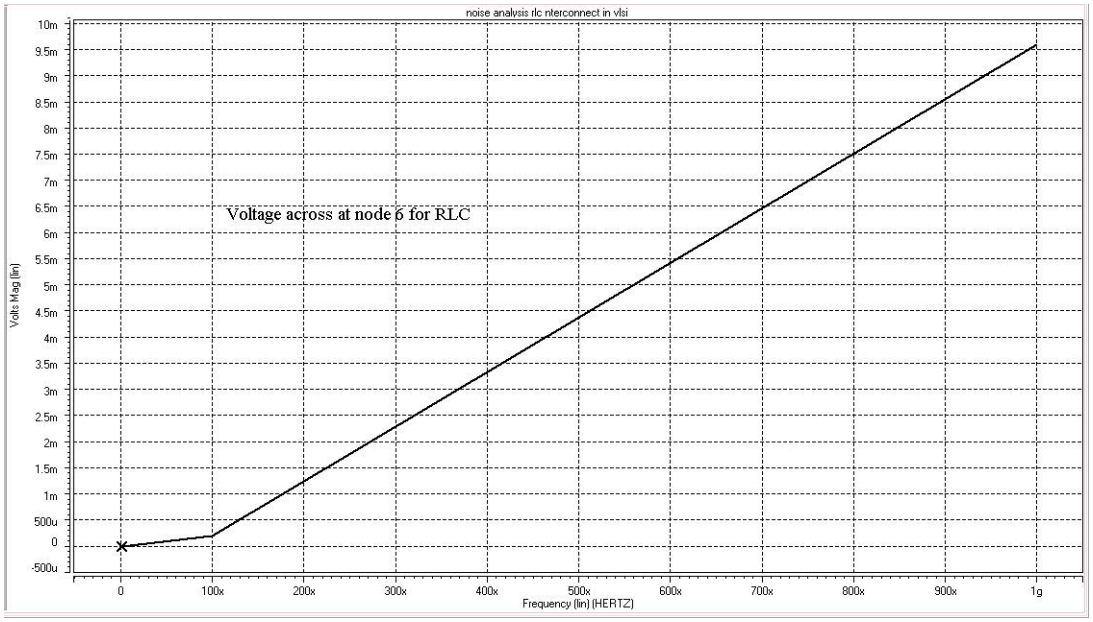


Fig. 13: Voltage in frequency domain across victim capacitor C_L at node 6 of Fig. 6(b) for 2π RLC interconnect, where R_d = 50 Ω, $R_s = R_{1a}$ = 20 Ω, $R_e = R_{1v}$ = 20 Ω, L_s = 302 nH, L_e = 302 nH, C_1 = 50 fF, C_2 = 100 fF, C_x = 150 fF and C_L = 10 fF

We perform the simulation program by HSPICE. Fig. 14 shows the output crosstalk noise voltage waveforms in frequency domain of RLC interconnect in DSM VLSI circuit for aggressor input reported by Sahoo et. el [3] and imported for Equation (17). While performing simulation by HSPICE, we use the maximum frequency of 1 Ghz. When the frequency is increasing, the noise voltage is decreasing gradually, as seen in the Fig. 14.

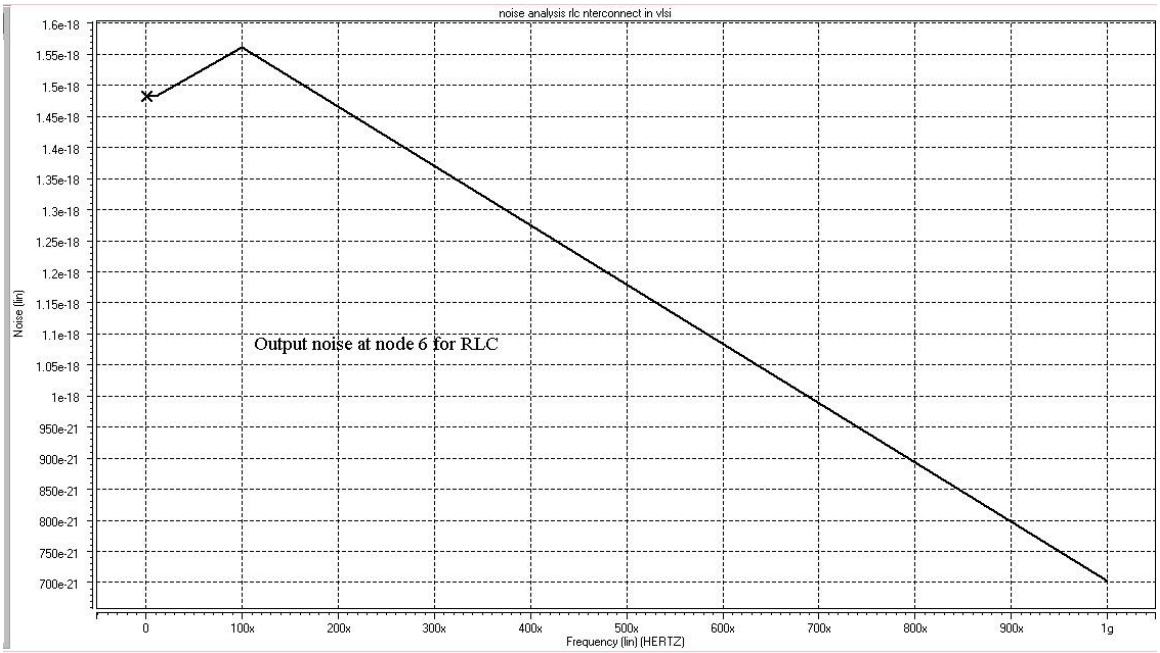


Fig. 14: Output crosstalk noise voltage waveform in frequency domain by HSPICE simulation for RLC interconnect, where R_d = 10 Ω, $R_s = R_{1a}$ = 10 Ω, $R_e = R_{1v}$ = 10 Ω, $L_s = L_{1a}$ = 0.5 nH, $L_e = L_{1v}$ = 0.5 nH, C_1 = 50 fF, C_2 = 100 fF, C_x = 150 fF and C_L = 5 fF

After simulation work, we calculated the peak values of the output crosstalk noise voltage using the Equation (20). The peak values of the output crosstalk noise voltage for both the calculated and simulated data are summarized in Table III. And then we compared the simulated data with the calculated data which are shown as % of error and % of average error in Table III. The table shows that the average % of error is 5.77%, which is good enough compared to the other results published in the literature [1], [3], [6], [11 – 14]. The comparison is shown in Table IV.

Table III: Comparison of Output Crosstalk Noise Peak Voltage for RLC Interconnect

Sl. No.	T_r (psec)	$R_d = R_{th}$ (Ω)	$R_{1a}=R_{2a}=R_{1v}=R_{2v}$ (Ω)	$L_{1a}=L_{2a}=L_{1v}=L_{2v}$ (nH)	$C_{la}=C_{lv}$ (fF)	Vpeak (μv) (HSPICE)	Vpeak (μV) Calculated	Error (%)	Average % Error
1	50	10	10	0.5	5	20.0236	18.27	8.749	**5.77**
2	100	50	20	1	10	34.1940	34.65	1.320	
3	150	100	50	10	15	51.5173	54.44	5.370	
4	**200**	**150**	**70**	**20**	**20**	**62.4839**	**67.41**	**7.300**	

Table IV: Comparison of Average % of Error for RLC Interconnect

	Our Work	Ref. [1]	Ref. [3]	Ref. [6]	Ref. [11]	Ref. [12]	Ref. [13]	Ref. [14]
	5.77	**6.8**	**4.89**	**57**	**4**	**5**	**20**	**<10**

IV. CONCLUSION

In this work, the output crosstalk noise voltages for both RC and RLC interconnects in DSM VLSI circuits are analysed and estimated. We use 10 GHz frequency for RC interconnects and 1 GHz frequency for RLC interconnects. In order to reduce output crosstalk noise, operating at 10 GHz and 1 GHz frequency for RC and RLC interconnect, respectively, are proposed along with 2π modelling approach. It is observed that the crosstalk noise is effectively reduced to 6.29% for RC interconnects and 5.77% for RLC interconnect with 2π modelling approach. These results are good enough compared to the other results published in the literature.

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