International Journal of Engineering Research and Development
e-ISSN: 2278-067X, p-ISSN: 2278-800X, www.ijerd.com
Volume 10, Issue 7 (July 2014), PP.41-45

VLSI Architecture for Optimized Low Power Digit Serial FIR Filter using MCM

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Abstract:- Many efficient algorithms and architectures for the design of low-complexity bit-parallel Multiple Constant Multiplications (MCM) operation that dominates the complexity of Digital Signal Processing (DSP) systems. On the other hand, digit-serial architectures offer alternative low-complexity designs, since digit-serial operators occupy less area and are independent of the data word length. This paper introduces the problem of designing a digit-serial MCM operation with minimal area at gate-level and presents the exact formalization of the area optimization problem In this paper, we address the problem of optimizing the area using multiple constant multiplier, design architecture. The proposed optimization algorithm is used in the design of digit-serial finite impulse response filters that will yield better performance, with high efficiency.

Keywords:- Digit Serial Adder, Fir filter, Multiple Constant Multiplications (MCM), Optimum Area, Power, Shift and Add Adder.

I. INTRODUCTION

Multiplication of a variable with a set of constants, also known as the MCM operation, is a central operation and performance bottleneck in many DSP applications such as, error correcting codes, linear DSP transforms, and Finite Impulse Response (FIR) filters. In hardware, the multiplication operation is considered to be expensive, as it occupies significant area. Hence, constant multiplications are generally realized using only addition, subtraction, and shift operations. For the bit-parallel design of the MCM operation, the MCM problem is defined as finding the fewest number of addition and subtraction operations that realize the MCM, since shifts can be implemented using only wires in hardware. Many efficient algorithms have been introduced for the MCM problem. In spite of various methods used and different search space explored, the main idea has always been the maximization of the sharing of common partial products among the constant multiplications. As an example, consider the constant multiplications 29x and 43x.

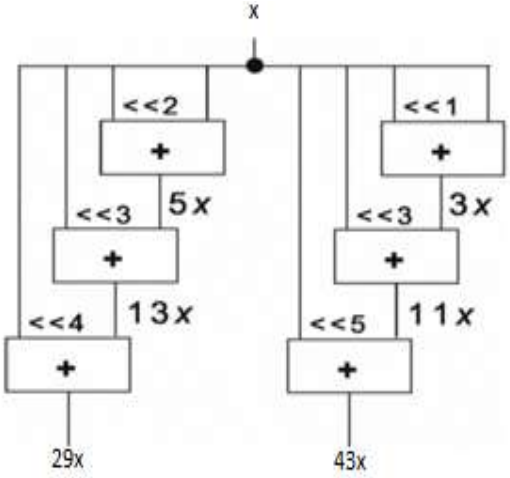

Fig. 1 (a)- Without Partial Product Sharing

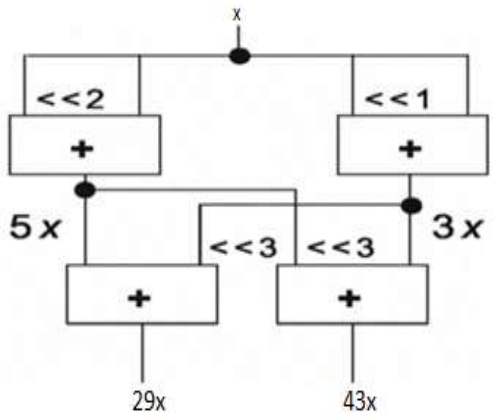

Fig. 1 (b)- With Partial Product Sharing

Observe from Fig. l (a) and Fig. 1 (b) that the sharing of partial products 3x and 5x reduces the number of operations from 6 to 4.

In digit-serial arithmetic, the words are divided into digit sets of d bits that are processed one at a time .The special cases of the digit-serial computation are called bit-parallel and bit-serial processing when the digit size d is equal to data word length and 1 respectively. The digit serial computation plays an important role when

the bit-serial implementations cannot meet delay requirements and the bit-parallel designs require excessive hardware. Thus, an optimal tradeoff between area and delay can be obtained by changing the digit size parameter (d).

The digit-serial MCM operation in shift-adds architecture consists of digit-serial addition and subtraction operations, and D flip-flops for the shift operations, as opposed to the bit-parallel MCM operation, where shifts are free in terms of hardware. The high-level algorithm aims to find a solution with the fewest number of additions, subtractions, and shift operations. To the best of our knowledge, there exists no algorithm that focuses on the minimization of area in digit-serial MCM operation at gate-level.

Here, we initially present the digit-serial realizations of addition, subtraction, and shift operations and determine their implementation costs in terms of gate-level metrics. Then, we introduce an exact algorithm that optimizes the area of the digit-serial MCM operation at gate-level. In the exact algorithm, all possible implementations of constant multiplications are found when constants are defined under a number representation and the optimization of area problem is formulated as a 0-1 ILP problem taking into account the hardware cost of each operation. Thus, the maximization of sharing of partial products and also the amount of shifts is realized based on a gate-level implementation. The experimental results indicate that the exact algorithm leads to low-complexity digit-serial MCM designs compared to those found by the exact algorithm designed for the MCM problem and those that are implemented using generic digit-serial multipliers.

II. LITERATURE REVIEW

1. An Algorithm for the Design of Low-Power Hardware-Efficient FIR Filters-2008[7]

Mustafa Aktan, Arda Yurdakul, and Günhan Dündar, *Member, IEEE*

This algorithm optimizes SPT terms in the coefficients given the filter frequency-response characteristics. Although the worst case run-time of the algorithm is exponential. The filters found by the proposed algorithm have fewer SPT terms and are shorter in word length than the filters found by the other methods.

2. Design and Implementation of Low Power Digital FIR Filter based on low power multipliers and adders on Xilinx FPGA -2011[8]

Bahram Rashidi Bahman Rashidi Majid Pourormazd

This paper presents the methods to reduce dynamic power consumption of a digital Finite Impulse Response (FIR) filter these methods include low power serial multiplier and serial adder, combinational booth multiplier,folding transformation in linear phase architecture and applied to fir filters to reduce power consumption.

3. Systematic Design of High-Speed and Low-Power Digit-Serial Multipliers – 1998[9]

Yun-Nan Chang ,

Janardhan H. Satyanarayana, Keshab K. Parhi.

These architectures can be pipelined at the bit-level, and as a result power can be reduced. The power consumed by a bit-serial design due to high-speed clock is much higher and this favors digit serial architectures with respect to low power consumption. Comparison of critical path and power consumption of different digit-serial multipliers and their variation with respect to digit sizes have been explored

4. Design of Digit-Serial FIR Filters: Algorithms, Architectures, and a CAD Tool -2013[10]

Khader Mohammad, Sos Agaian

In this paper, we introduced the 0–1 ILP formalization for designing digit-serial MCM operation with optimal area at the gate level. They also proposed an approximate GBalgorithm that finds the best partial products in each iteration which yield the optimal gate-level area in digit-serial MCM design.

5. Low Power Implementation of Decimation Filters in Multistandard Radio Receiver Using Optimized Multiplication-Accumulation Unit -2007[12]

Nadia Khouja, Khaled Grati, Adel Ghaze

In this work, the implementation of decimation filters for multistandard wireless transceivers was optimized to reduce its power consumption. The power reduction is achieved through the usage of a MAC unit inside the filters that reduce the total activity and therefore the dynamic power. The multiplication function of the MAC unit is based on the Radix-4 modified-Booth algorithm for the generation of the partial products. For summation, carry save addition was used. A Pipeline stage is then introduced.

III. PROPOSED ARCHITECTURE

The designing digit serial arithmetic operation with optimal area at the gate level by considering the implementation cost of digit serial addition, subtraction and shift operation is one of the most important parameter. Realization of digit-serial FIR filters under the shift-adds architecture for area reduction compare to the filter designs whose multiplier blocks using digit-serial constant multipliers and power reduce by using the high-level optimization algorithms is proposed here by Digit-Serial FIR Filter.

IV. PROPOSED ALGORITHM

Digit serial FIR Filter for low power can be designed using 1.Multiple Constant Multiplier with Shift and Add algorithm Filter implementation has concentrated on implementation using various VLSI technologies .Finite Impulse Response (FIR) filters are of great importance in Digital Signal Processing (DSP) systems since their characteristics in linear-phase and feed-forward implementations make them very useful for building stable high-performance filters. The direct and transposed-form FIR filter implementations are illustrated in Fig. 1(a) and (b), respectively. Although both architectures have similar complexity in hardware, the transposed form is generally preferred because of its higher performance and power efficiency [1]. The multiplier block of the digital FIR filter in its transposed form [Fig. 1(b)], where the multiplication of filter coefficients with the filter input is realized, has significant impact on the complexity and performance of the design because a large number of constant multiplications are required and is also a central operation that has performance bottleneck in many other DSP systems such as fast Fourier Transforms, Discrete Cosine Transforms (DCTs), and error-correcting codes. In several cases it is senseless to use conventional bit-parallel circuits: their implementations have an important cost in area and run faster than the speed needed by the application. In this way, digit-serial architectures become an important alternative to efficiently implement a wide range of real time signal processing circuits. The digit-serial approach allows the designer to select an intermediate area-time, situated between the bit-parallel and the bit-serial implementations. However, the digit-based recoding technique does not exploit the sharing of common partial products, which allows great reductions in the number of operations and, consequently, in area and power dissipation of the MCM design at the gate level. Hence, the fundamental optimization problem, called the MCM problem, is defined as finding the minimum number of addition and subtraction operations that implement the constant multiplications. Note that, in bit-parallel design of constant multiplications, shifts can be realized using only wires in hardware without representing any area cost.

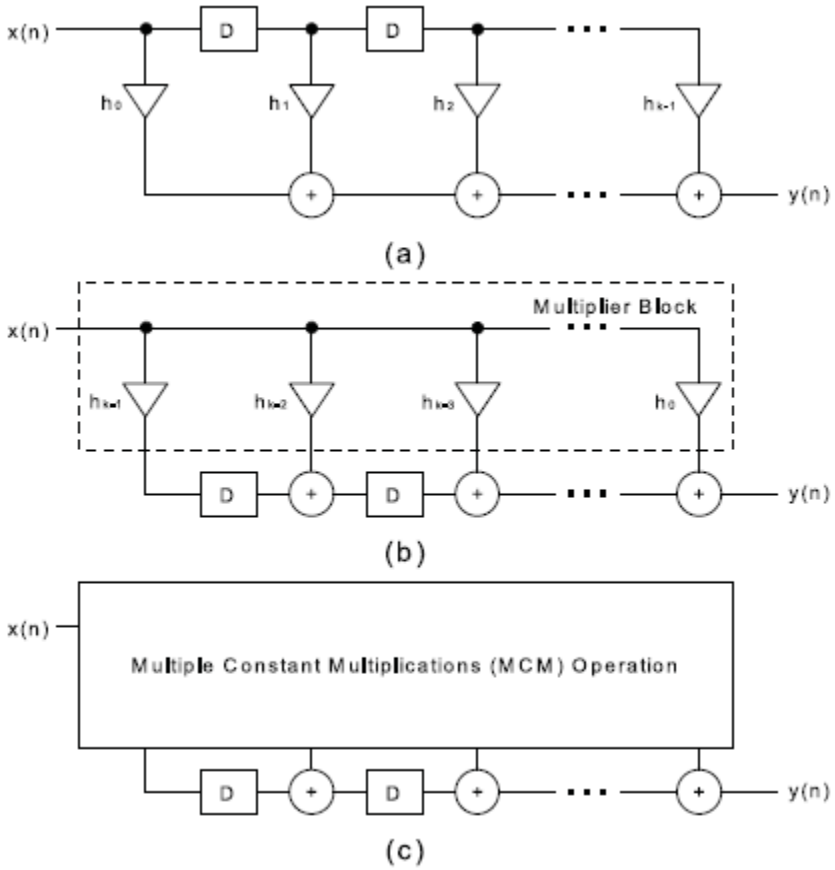

Fig. 2:FIR filters implementations. (a) Direct form. (b) Transposed form with generic multipliers. (c) Transposed form with an MCM block.

Multiplication with a constant is commonly used in digital signal processing (DSP) circuits, such as digital filters. The transfer function of an Nth-order finite- length impulse response (FIR) filter can be written as

In a transposed direct form FIR filter, one input is multiplied with multiple coeffi- cients [11],[12]. This is often referred to as the multiple- constant multiplication (MCM) problem, which can be realized using a multiplier block as illustrated by the dashed box in Fig. 2(b). Constant multiplication can be efficiently implemented using shifts, adders, and subtracters. As the complexity is similar for adders and subtracters we will refer to both as adders, and the number of adders and subtracters as adder cost. Each multiplier in a multiplier block can be implemented separately, e.g. using the canonic signed-digit (CSD) representation [11],[32]. However, it is possible to utilize redundant partial results to reduce the number of adders required to realize multiple-constant multiplication [14]–[15]. Most existing work on MCM has focused on mini- mizing the number of adders, as the shift operations can be hardwired in a bit-parallel architecture. Howev- er, in bit- and digit-serial arithmetic the shift opera- tions require flip-flops, and, hence, they have to be considered as well. In [15] an algorithm that minimiz- es the number of shifts while keeping the adder cost low was proposed.

Most work on implementation of digit-serial FIR filters has focused on implementation in FPGAs and without using multiplier blocks [16]–[18]. However, in [19] the digit-size trade-off in implementation of digit-serial transposed direct form FIR filters using multiplier blocks was studied.

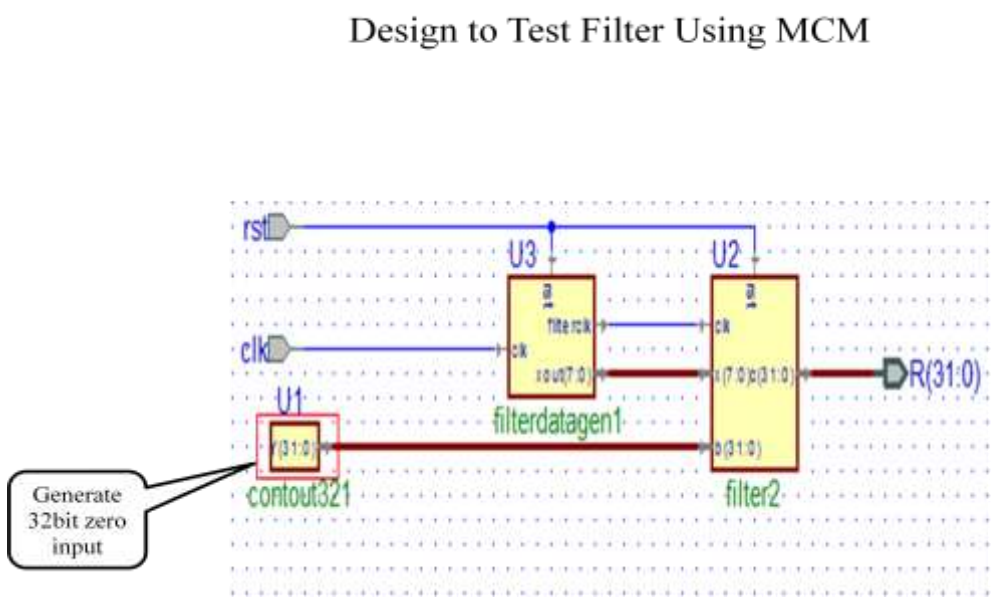

Fig. 3 (a)- Fliter using MCM

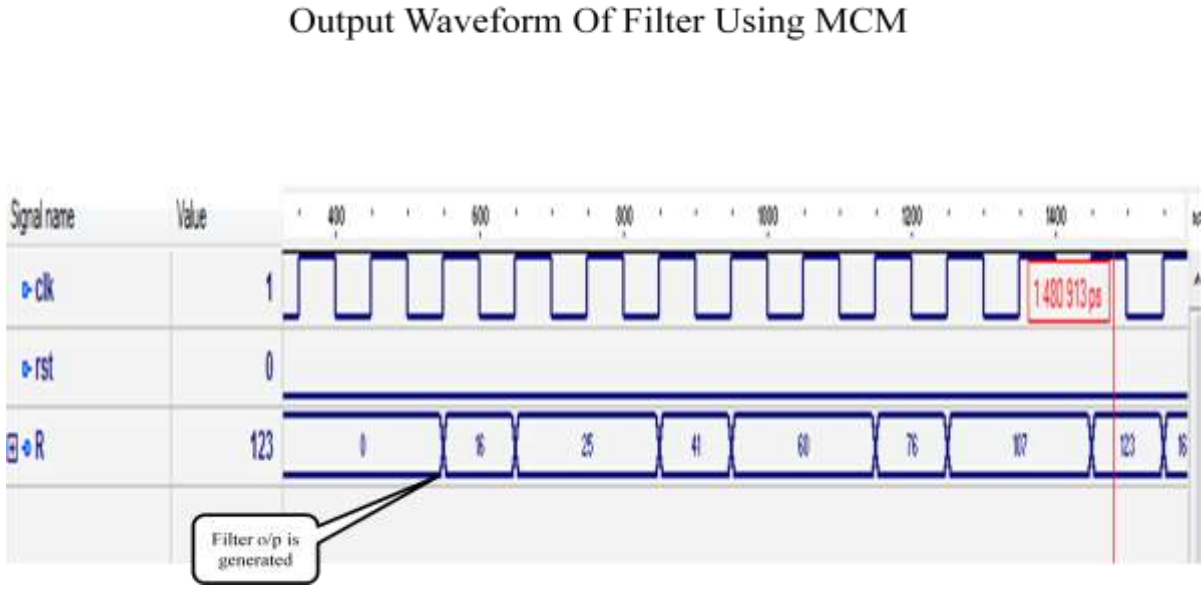

Fig. 3 (b) Output Waveform of Flite using MCM

V. CONCLUSIONS

In this paper implementation of low power digit-serial FIR filters using multiple constant multiplication (MCM) techniques has been considered. Some con- clusions regarding design guidelines for low power digit-serial multiplier blocks can be deduced. The ac- tual complexity in terms of adder cost and number of shifts is not the main factor determining the power consumption. Instead the adder depth, as for parallel arithmetic, is a main contributor. Hence, an algorithm with low adder depth should be used. Furthermore, the shifts prevent glitch propagation through subsequent adders. For even coefficients the shifts can be placed either before or after the final additions. Hence, a heu- ristic for placing the shifts would be also useful.

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[8]. This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS

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