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# A New Hybrid 27-Level Cascaded Multilevel Inverter Fed Induction Motor Drive With Low Common Mode Voltage

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**Abstract*:-*** Hybrid cascade multilevel inverters combine semiconductor devices of different voltage ratings and technologies, which theoretically allow high efficiency to be achieved. This paper deals with new hybrid multilevel inverter fed induction motor drive. It focuses on asymmetrical topologies, and introduces 27-level inverter fed Induction motor drive. The total harmonic distortion (THD) is reduced with more number of steps in output voltage without using pulse width modulation techniques. A new method is proposed to reduce the common mode voltage and bearing currents. This paper also focuses on the voltage balancing. Simulation results obtained from Matlab/simulink to simulate 27-levels of voltage and the parameters of the drive.

**Keywords:-** Cascaded multilevel inverter, Induction motor drive, Common mode voltage, Bearing currents, Total harmonic distortion.

## I. INTRODUCTION

In recent years multilevel inverters have became a very interesting field of study in what regards their industrial application. These converters allow the synthesizing of a sinusoidal voltage waveform starting from several levels of dc voltages. However, besides that advantage there are other important advantages such as, reduced switching losses, low dv/dt's and reduced common mode voltages. Due to these characteristics several multilevel inverter topologies have been developed and studied.

Recent advances in power switching devices enabled the suitability of multilevel inverters for high voltage and high power applications because they are connecting several devices in series without the need of component matching. Cascaded H-Bridge inverters can be classified into two types based on the amplitudes of the DC sources used. They are: symmetrical multilevel inverters in which sources are of equal amplitudes and asymmetrical multilevel inverters in which sources are of different amplitudes. Compared to symmetrical multilevel inverter it can be seen that asymmetrical multilevel inverters can generate more voltage levels and higher maximum output voltage with the same number of bridges. The asymmetric multilevel inverter can produce $N=2^{n+1}-1$, levels (n is the number of sources and N is the number of levels in the inverter output). The main advantage of the asymmetric configuration is that if minimizes the redundant output levels.

The outputs of dc–ac converters contain common-mode voltage switched at high frequencies with voltage magnitudes that are comparable to the inverter pole voltages. High frequency switching of the common-mode voltage in the induction motor causes several issues like leakage currents through the stray capacitance between the winding and the body of the motor and create shaft voltages causing bearing currents resulting in bearing failures of the motors[3]–[6].

The effects of common-mode voltage are much more adverse in the case of medium- and high-voltage drives due to high frequency switching of common-mode voltage in the order of few kilovolts. High *dV*/*dt* switching in common-mode voltage causes breakdown of bearing lubricant insulation and causes pitting in the bearing surfaces. This leads to quick failure of bearings.

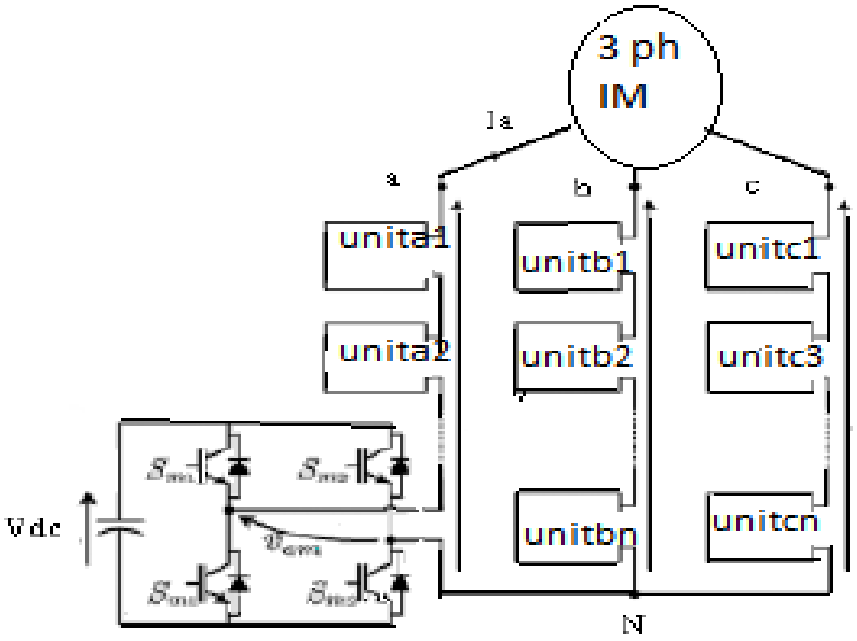



**Fig. 1 Basic new hybrid inverter scheme.**

The inverter $3^s$ different voltages (e.g. an inverter with s=3 cells can generate $3^3$=27 different voltage levels. The basic new hybrid inverter structure for one phase is shown in fig:1. This multilevel inverter consists of series connected cells. Each cell consists of a 4-switch H-bridge voltage source inverter. The output inverter voltage is obtained by summing the cell contributions.

## I.PROPOSED TOPOLOGY

In the proposed topology, the magnitude of the dc voltage sources differs from one unit to another.

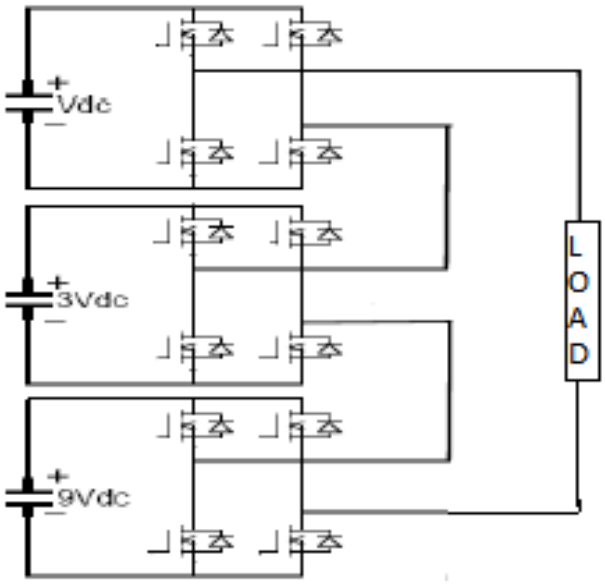



**Fig. 2: Proposed new hybrid inverter scheme for 27 level output voltage.**

The new Hybrid multilevel inverter consists of full bridge modules which have the relationship of 1v,3v,9v….$3^{n-1}$ for dc link voltage. The output waveform has 27 levels. The following table.1 shows the appropriate switching sequence of getting 27 level output voltage at the inverter terminals.

**Table. I. Switching sequence of cascaded multilevel inverter for 27 level output voltage.**

| V out | 1Vdc | 3Vdc | 9Vdc |
|---|---|---|---|
| -13 Vdc | N | N | N |
| -12 Vdc | O | N | N |
| -11 Vdc | P | N | N |
| -10 Vdc | N | O | N |
| -9 Vdc | O | O | N |
| -8 Vdc | P | O | N |
| -7 Vdc | N | P | N |
| -6 Vdc | O | P | N |
| -5 Vdc | P | P | N |
| -4 Vdc | N | N | O |
| -3 Vdc | O | N | O |
| -2 Vdc | P | N | O |
| -1 Vdc | N | O | O |
| 0 Vdc | O | O | O |
| +1 Vdc | P | O | O |
| +2 Vdc | N | P | O |
| +3 Vdc | O | P | O |
| +4 Vdc | P | P | O |
| +5 Vdc | N | N | P |
| +6 Vdc | O | N | P |
| +7 Vdc | P | N | P |
| +8 Vdc | N | O | P |
| +9 Vdc | O | O | P |
| +10Vdc | P | O | P |
| +11Vdc | N | P | P |
| +12Vdc | O | P | P |
| +13Vdc | P | P | P |

## II. REDUCTION OF COMMON MODE VOLTAGE

The common-mode voltage is an average of the phase voltages. The common-mode voltage, and especially rapid changes in it, is one of the reasons for bearing currents in the drives, and is therefore harmful. A rapid change in the common-mode voltage is induced in the motor every time when only one of the phases changes its output voltage level. If the motor terminal voltage oscillates after the switching, the common-mode voltage will also oscillate. With multilevel inverters, it is possible to arrange the phase voltages so that the common mode voltage will be zero at all times. This is based on the fact that some nodes on the voltage hexagon lattice have such redundant switching states that the sum of the phase voltages is zero. The new method proposed here to keep common mode voltage zero is given by parallel phase topology.

### A. Parallel phase topology

Since nearly all multilevel inverters involve effective series connection of transistor devices, parallel connection of inverter poles through inter-phase reactors. However, the multilevel features and redundancy were noted by researchers some time ago. One advantage of parallel connection is that the devices share current and this topology is good for high current loads. It is also reasonable to perform parallel combinations of diode-clamped poles so that the transistor voltage and current ratings are reduced. This structure has the advantage of providing a high number of voltage levels while reducing the voltage and current stress on the individual transistors and hence the common mode voltage oscillations are low with proper voltage balancing. Fig. 3 shows a three-phase inverter made from parallel two-level poles.

The inter-phase reactor is similar to a typical transformer with the exception that an air-gap exists in the core to ensure linearity and the windings are such that the resistance and leakage inductances are small. With these assumptions, the reactor will have equal voltages on each half meaning that the line-to-ground voltage is the average of that of each of the two-level poles. Then the general relationships for the *a*-phase can be listed as in Table-II.

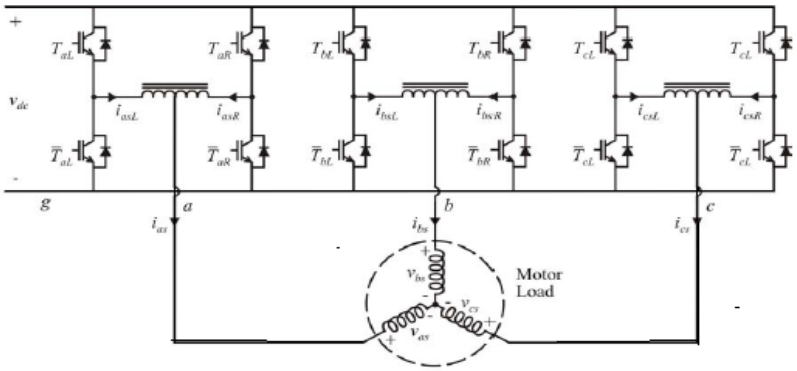



**Fig. 3 Parallel phase multilevel inverter topology**

**Table. II. Parallel inverter relationships.**

| Sa | TaL | TaR | Vag | iadc |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | Vdc/2 | iasR |
| | 1 | 0 | Vdc/2 | iasL |
| 2 | 1 | 1 | Vdc | ias |

The *a*-phase line-to-ground voltage can be expressed in terms of the transistor signals by

$$Vag=1/2(TaL+TaR)Vdc \qquad (1)$$

For ideal operation, the reactor currents should be equal *iasR = iasL* . In practice, this is easy to ensure since the redundant states can be selected to drive the common mode reactor current to zero. To understand the operation of the inter-phase reactor, it can be replaced by the model shown in Fig. 4.

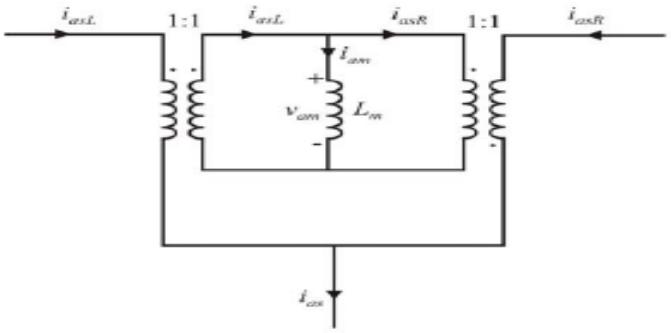



**Fig. 4 Model of inter-phase reactor**

This model is derived from the standard transformer model with the resistance and leakage inductance set to zero. As it turns out, the transformer model is better suited for the reactor since the reactor contains an air-gap yielding negligible core losses. The 1:1 transformers in Figure:4 are ideal and thus ensure that each side of the reactor will have the same voltage. This magnetizing voltage can be expressed in terms of the transistor signals and dc voltage as

$$Vam=1/2(TaL-TaR)Vdc \qquad (2)$$

From (2), the magnetizing current can be calculated by

$$P.iam=Vam/Lm \qquad (3)$$

Once the magnetizing current is known, the left and right reactor currents can be found by solving the two unknowns from the two KCL equations

$$\text{Ias L-iasR=iam} \qquad (4)$$

$$\text{Ias L+iasR=ias} \qquad (5)$$

Considering (2), it can be seen that the redundant states in Table-1 can make the magnetizing voltage positive or negative effecting the change in *iam* according to (3). This can be used to control *iam* to zero yielding zero common mode current according to (4) so that *iasR* = *iasL* . It should be pointed out that the material presented herein shows the fundamental example. Extensions of this material include paralleling multi-level phases, combining the parallel topology with an H-bridge structure, and paralleling more than two phases.

**B. Reactor current sharing:**

For the parallel topology shown in Figure 3, the redundant states can be used to ensure current sharing in the reactor. The digital flag input for the *a*-phase is

$$I_{aLR} = \begin{cases} 1 & i_{asL} > i_{asR} \\ 0 & i_{asL} \le i_{asR} \end{cases}$$

Similar current sharing flags are defined for the *b*- and *c*-phase. In this topology, the lowest *sa* = 0 and highest *sa* = 2 switching states do not affect the reactor current balance. This is fortunate, since there is no redundancy available for these states. The middle state affects the reactor current sharing, but has redundancy according to Table-1. The redundant choice to be placed in the RSS table is straightforward according to the discussion in the previous section about the inter-phase reactor. Specifically, the transistors can be set to *TaR* = *IaLR* and *TaL* = 1− *I aLR* when *sa** = 1.

The load was a 20 kW induction motor operating at rated power. As can be seen, the left and right side of the reactor share the phase current equally. At one point in the study, the RSS is turned off and only one of the redundant states is used. As can be seen, the reactor currents become unbalanced until the RSS is turned on again. Another method of switching this type of inverter is to alternate back and forth between the redundant states. In this case, the balance will be decent, but there will be some drift from the perfect current sharing case. Therefore, an active RSS control is recommended.

## III. ACTIVE VOLTAGE BALANCING

The way the individual DC sources are synthesized to construct the cumulative inverter output voltage using staircase modulation method. If the same pattern of duty cycles is used on a motor drive continuously, then one battery is cycled on for a much longer duration than another thus discharging sooner. Since the switches do not share the same load during the construction of the multi level waveform, the gate triggering of these switches must be rotated to actively share the duty cycle. However, by using a switching pattern swapping scheme among the various levels, all batteries will be equally used charged and/or discharged. The combination of the 180° conducting method or staircase modulation method and the pattern-swapping scheme make the cascade inverter's voltage and current stresses the same and battery voltage balanced.

## IV. EXPERIMENTAL RESULTS

The Matlab/Simulink model of the proposed inverter for 27 level output is shown in Figure.5. Simulation is performed for the proposed circuit with MATLAB/SIMULINK. It is clear that as the number of level increases, distortion reduces as shown in the figure.6 (a) and (b).

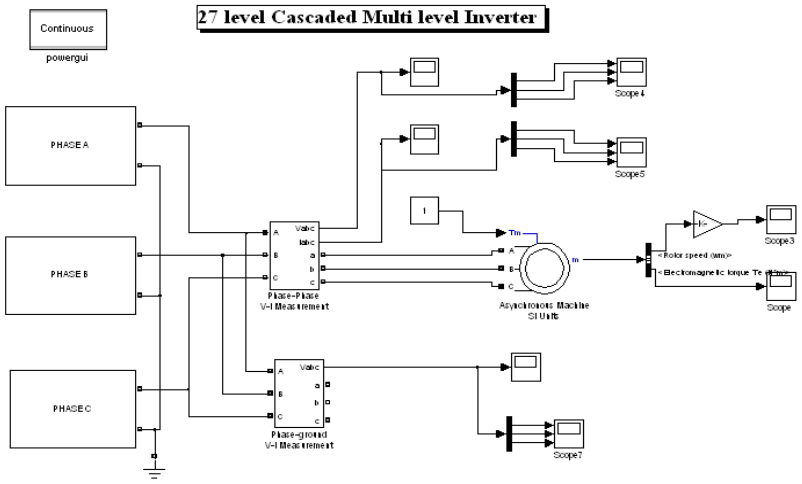
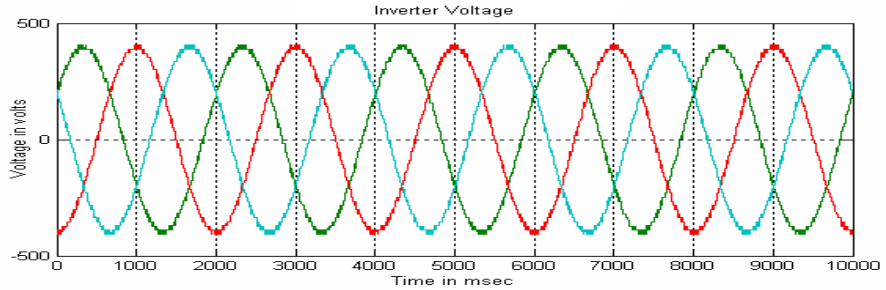
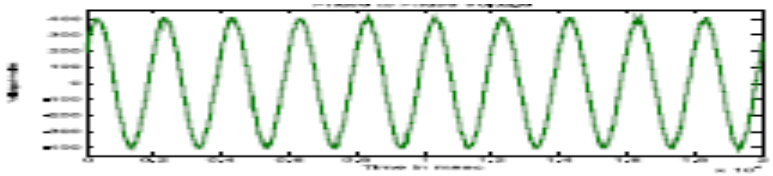


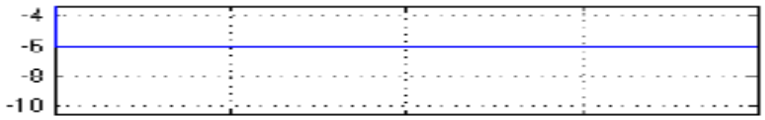

**Fig. 5 Simulation diagram of proposed system.**




**(a)**



**(b)**




**(c)**

**Fig. 6 (a) Three phase output voltage of Multilevel inverter.(b) Line voltage waveform. (c) Common mode voltage in the 27 level inverter.**

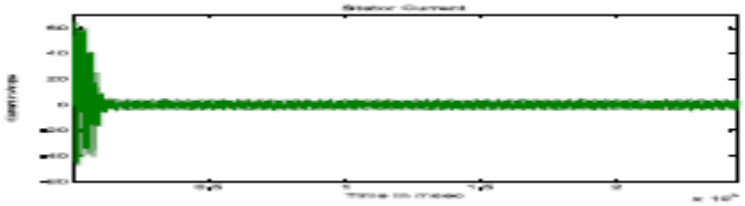


**Fig. 7 Stator current waveform of motor**

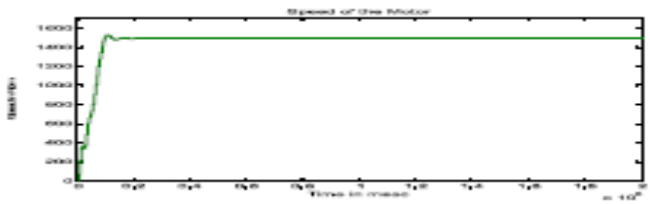


**Fig. 8 Speed of motor**

## V. CONCLUSION

In this paper a new topology is presented to reduce the common mode voltage, shaft voltages and bearing currents, without the use of PWM techniques. The most important feature of the system is being convenient for expanding and increasing 27 number of output levels with very low harmonic content which theoretically allow high efficiency to be achieved. This paper also focuses on the voltage balancing which plays an important role when we are dealing with the asymmetric topologies. Simulation results were obtained from Matlab/simulink to simulate 27-levels of output voltage and the parameters of the drive.

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