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Design of Low Power High Speed Fully Dynamic CMOS Latched Comparator

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Abstract: A novel of low power high speed comparator is proposed in this paper which consists of less sensitive in delay using dynamic CMOS latched comparator method. It aimed for less sensitive in delay and high speed design compared with other design techniques. The simulation results carried out using LT spice tool shows up to 62% less sensitivity of the delay, which is about 0.098ns than the conventional double-tail latched comparators at approximately the same area and power consumption.

I. INTRODUCTION

Due to fast-speed, low-power consumption, high-input impedance and full-swing output, CMOS dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time. However, an input-referred latch offset voltage (hence offset voltage), resulting from the device mismatches such as threshold voltage V_{th}, current factor $\beta(=\mu C_{ox}W/L)$ and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators [1], [2]. Because of this reason, the input-referred latch offset voltage is one of the most important design parameters of the latched comparator. If large devices are used for the latching stage, a less mismatch can be achieved at the cost both of the increased delay (due to slowing the regeneration time) and the increased power dissipation.

More practically, the input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output-latch stage as shown in Fig 1. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise [3]. However, the pre-amplifier based comparators suffer not only from large static power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance r_{ds} due to the continuous technology scaling [4].

The various types of the comparators can be classified in to three: Open-loop Comparators (op-amps without compensation), Pre-amplifier Based Latched Comparators (open-loop comparator combined with dynamic regenerative latch), and Fully Dynamic Latched Comparator. In this paper, various kinds of fully dynamic latched comparators will be fully analyzed in terms of their advantages and disadvantages along with operating principles and experimental results of the speed, delay ,power consumption at a limited area.

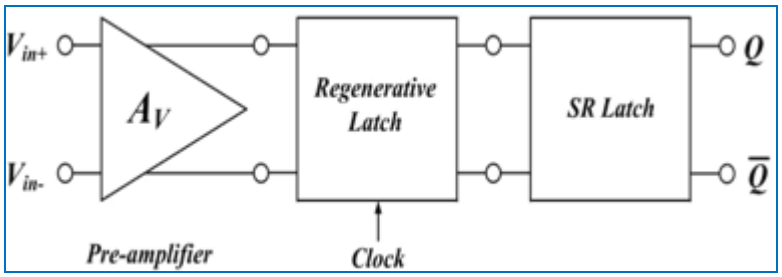

Fig 1: Typical block diagram of a high-speed voltage comparator.

II. LITERATURE SURVEY

In the literature, a few dynamic comparators can be found, such as Resistor divider (or Lewis-Gray) [5], Differential pair [6], double tail latch type SA [7]-[8], however, very little emphasis is placed on actual details of operation of these structures [5]. In this paper various comparator deals about how non-idealities due to process variation affect these structures along with experimental results to comparison of delay of different structures [1] with the different load capacitance of 7fF and 10fF. These experimental values varies in ns. However, the literature is devoid of any information on how other non-idealities such as imbalance in parasitic capacitors, common mode (CM) voltage errors or clock timing errors affect these structures. The operation and the effects of non-idealities of such dynamic comparators have been explore in this paper. A new dynamic

comparator structure which achieves a less propagation delay has been developed. In the new comparator structure, inputs are reconfigured [2]-[4] from the typical differential pair comparator [6] so that each differential pair branch contributes equal current at the meta stable operating point (or trip point) along with keeping the differential pair's tail current in saturation region. Comparison of the new architecture with respect to typical differential pair structure [6] is made as both structures share the same base structure.

III. COMPARATOR ARCHITECTURES

3.1 Open loop comparator

Open-loop, continuous time comparators are an operational amplifier without frequency compensation to obtain the largest possible bandwidth, hence improving its time response. Since the precise gain and linearity are of no interest in comparator design, no-compensation does not pose a problem. However, due to its limited gain-bandwidth product, open-loop comparators are too slow for many applications. One the other hand, a cascade of open-loop amplifiers usually has a significantly larger gain-bandwidth product than a single-stage amplifier with the same gain. However, since it costs more area and power consumption, cascading does not give practical advantages for many applications.

3.2 Regenerative comparator

Regenerative comparators (latches) use positive feedback to accomplish the comparison of two signals. Fig 2 and Fig 3 shows basic NMOS latch and PMOS latch . Latches have a faster switching speed and the propagation delay of the regenerative comparator is slow at the beginning and speeds up rapidly as time increases.

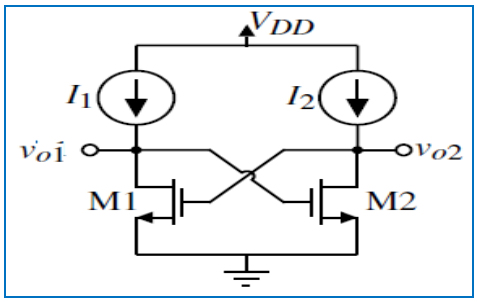

Fig 2: NMOS Latch

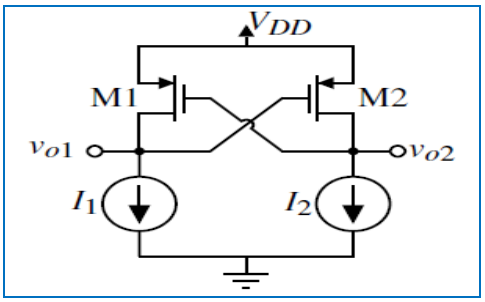

Fig 3: PMOS Latch

3.3 High speed comparator

High speed comparator consists of open loop and regenerative comparator. It mainly consist of three blocks, Input stage, a flip flop and S R latch. It uses a preamplifier to build up the input change to a sufficiently large value and then applying it to the latch. This architecture combines the best aspects with a negative exponential rise due to preamplifier stage and positive exponential rise due to latch stage. The main advantage of high speed comparator have a propagation delay as low as possible and faster response.

IV. FULLY DYNAMIC CMOS LATCHED COMPARATOR

4.1 Dynamic Latch

A dynamic latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. A simple dynamic latch is shown in Fig 4.The circuit is driven by a clock. During one phase of the clock (clk =1) when the transmission gate is closed, the latch acts transparent, and the inverter is directly connected to the input. In the other phase of the clock (clk = 0), the transmission gate opens and the inverter's output is determined by the node. Setup and hold times determined by the transmission gate must be taken in consideration in order to ensure proper operation of the latch i.e. adequate level of voltage is stored on the gate capacitance of the latch.

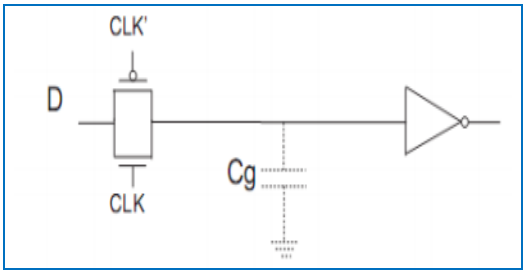

Fig 4: Dynamic Latch

4.2 Resistor Divider Comparator (or Lewis-Gray Comparator)

Fig 5 shows the Lewis-Gray comparator. Since the input transistor M1A/B and M2A/B operate in the triode region and act like voltage controlled resistors, this comparator is called "Resistive Divider Comparator." The advantage of this comparator is its low power consumption (No DC power consumption) and adjustable threshold voltage (decision level) since Lewis-Gray comparator shows a high offset voltage and its high offset voltage dependency on a different common mode voltage V_{com}, it is only suitable for low resolution comparison.

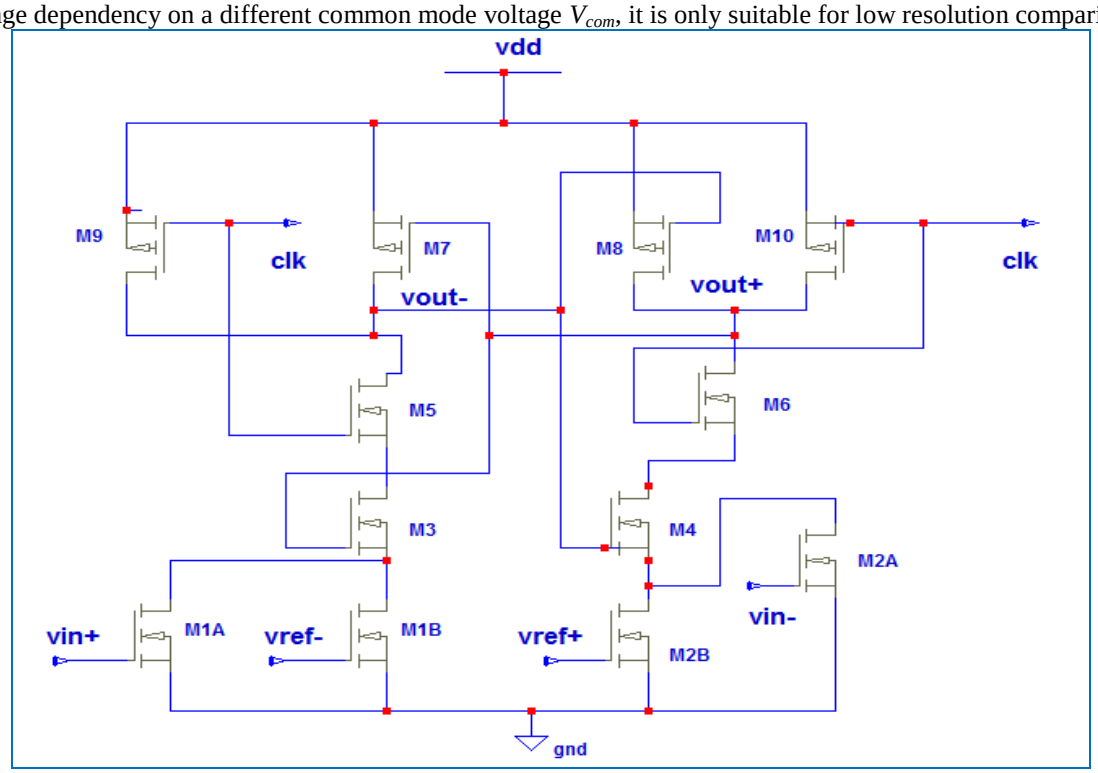

Fig 5: Lewis-Gray Comparator.(Comparator1)

4.3 Latch-type Voltage SA

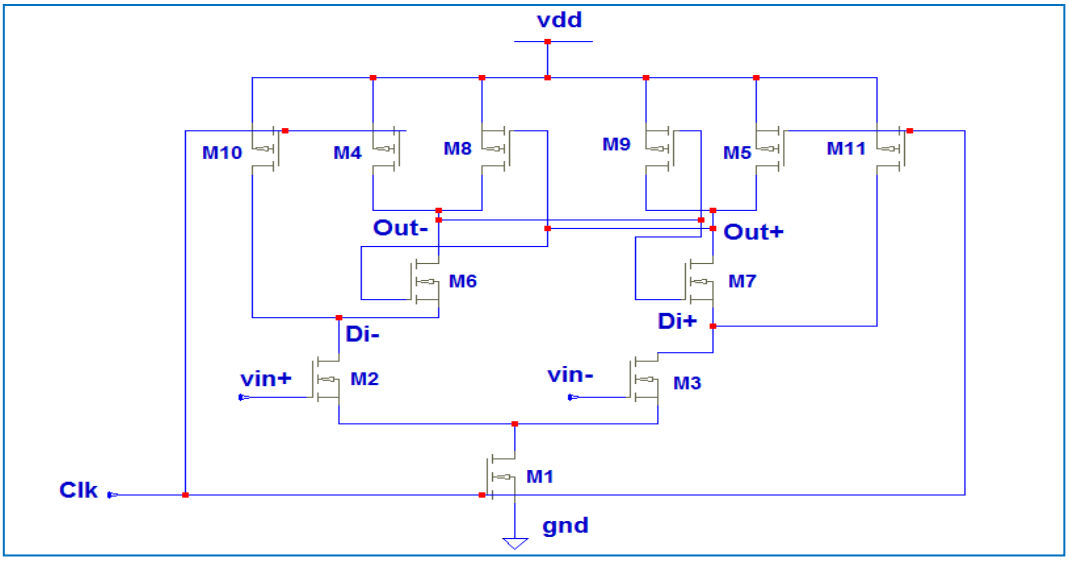

Fig 6: Latch-type Voltage SA .(Comparator2)

Comparing with Lewis-Gray comparator, Latch-type SA comparator shows faster operation and less overall offset voltage. The Fig 6 shows latch -type voltage SA However, still its structure which consists of a stack of 4 transistors requires large voltage headroom and it is problematic in low-voltage deep-submicron CMOS technologies .In addition, since it shows the strong dependency on speed and offset voltage with a different common-mode input voltage V_{com} [6], and it has less attractive in applications with wide common-mode ranges such as ADCs [7].

4.4 Double-Tail Dynamic Latched Comparators

To mitigate the drawbacks (strong dependency on speed and offset with a different common-mode input voltage V_{com} and problem in low power supply voltage operation due to its structure: a stack of four transistors) from the comparator shown in Fig 6, a comparator with separated input-gain stage and output-latch stage, shown in Fig 7.This separation made this comparator have a lower and more stable offset voltage over wide common-mode voltage (V_{com}) ranges and operate at a lower supply voltage (V_{DD}) as well.

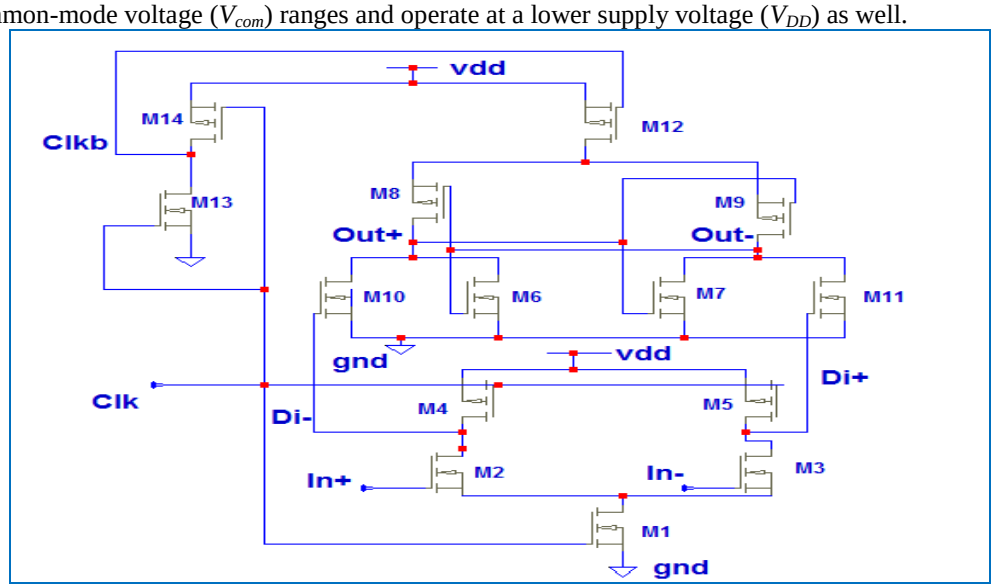

Fig 7: Double-Tail Dynamic Latched Comparators.(Comparator3)

4.5 Operation Principles of Proposed Comparator

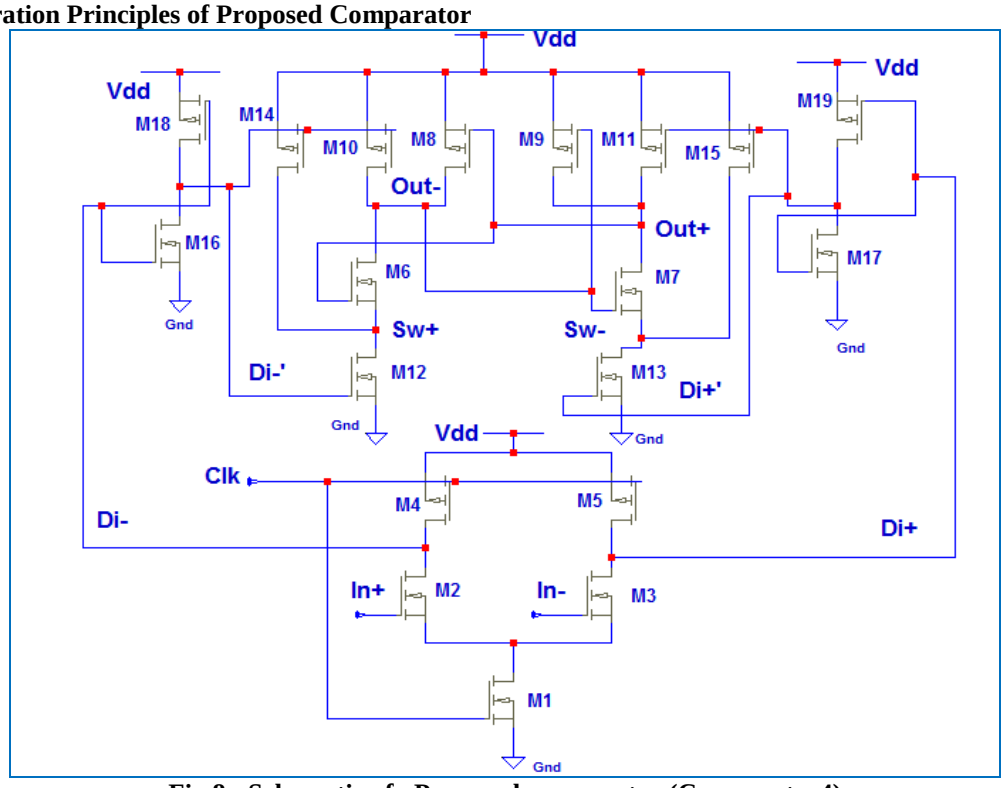

Fig 8 : Schematic of Proposed comparator.(Comparator4)

The schematic circuit diagram of the proposed comparator is shown in Fig 8.The proposed comparator provides better input offset characteristic and faster operation in addition to the advantages of those comparators such as less kickback noise, reduced clock load and removal of the timing requirement between *Clk* and *Clkb* over a wide common-mode and supply voltage range.

For its operation, during the pre-charge (or reset) phase (*Clk*=0V), both PMOS transistor M4 and M5 are turned on and they charge *Di* nodes' capacitance to V_{DD}, which turn both NMOS transistor M16 and M17 of

the inverter pair on and *Di'* nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 and M15 are turned on and they make Out nodes and *Sw* nodes to be charged to V_{DD} while both NMOS transistors M12 and M13 are being off.

During the evaluation (decision-making) phase ($Clk=V_{DD}$), each *Di* node capacitance is discharged from V_{DD} to ground in a different time rate in proportion to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between *Di+* and *Di-* node. Once either *Di+ or Di-* node voltage drops down below around V_{DD} - $|V_{tp}|$,the additional inverter pairs M18/M16 and M19/M17 invert each *Di* node signal into the regenerated (amplified) *Di'* node signal. Then the regenerated and different phased *Di'* node voltages are amplified again and relayed to the output-latch stage by transistor M10−M13. As the regenerated each *Di'* node voltage is rising from 0V to V_{DD} with a different time interval (or a phase difference, which increases with the increasing input voltage difference V_{in}), M12 and M13 turn on one after another and the output-latch stage starts to regenerate the small voltage difference transmitted from *Di'* nodes into a full-scale digital level: *Out+* node will output logic high (V_{DD}) if the voltage difference at *Di'* node*s Di'(t)* is negative *(Di+'(t)< Di-'(t)*) and *Out+* will be low (0V) otherwise. Once either of the *Out* node voltages drops below around V_{DD} - $|V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.

V. SIMULATION RESULTS

The various comparator circuits are designed and simulated with LT SPICE using 180nm PTM (Predictive technology Model) and the design circuits operated at **1V** power supply. Outputs of the different comparators shown in Fig:9,10,11 & 12

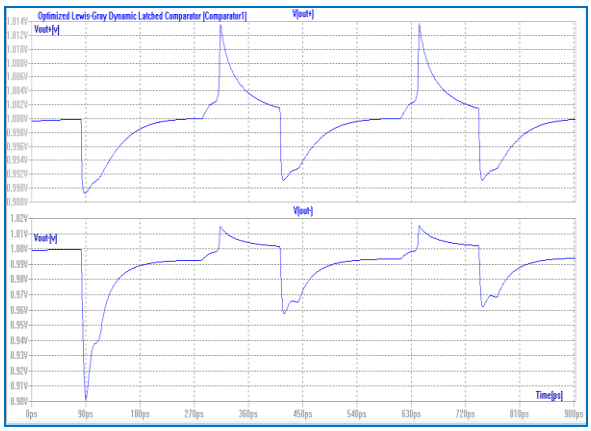

Fig 9 :Lewis-Gray Dynamic Latched Comparator (Comparator1)

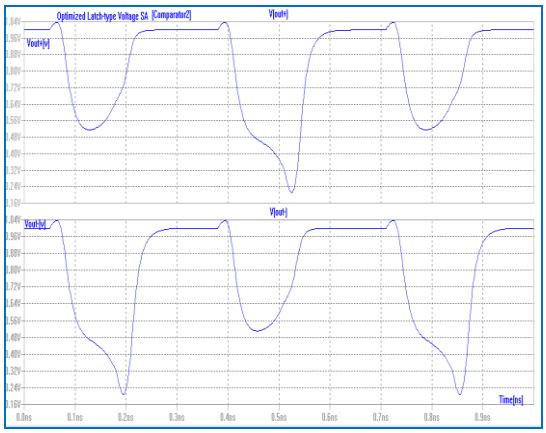

Fig 10:Latch-type Voltage SA (Comparator 2)

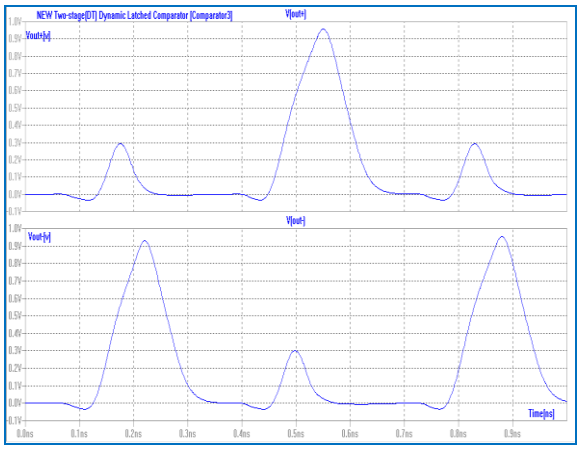

Fig 11 : Double-Tail Dynamic Latched Comparator (Comparator3)

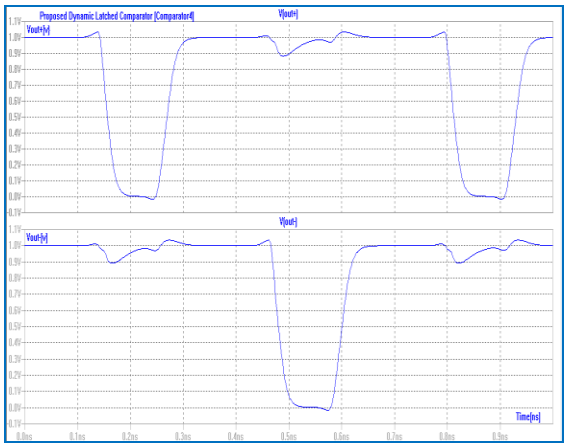

Fig 12: Proposed Dynamic Latched Comparator (Comparator4)

To compare the performances of the proposed comparator with other comparators , each circuit was designed using 180 nm PTM technology with $V_{DD}=1V$ and simulated with SPICE. The simulation results shown in table 1.In order to compare their relative speeds with less sensitive in delay multi-stage

dynamic comparators (Comparator3 and Proposed Comparator4) which has a separate input-stage and output-latch stage were designed to have the same $C_{Di}/I_{D2,3}$ (*Di* nodes capacitance/drain current of M1 and M2) ratio at the same area. All sizes of the input transistor pairs were designed as W/L (=2µm/0.12 µm) to have a relatively the same transconductance and offset voltage, which causes the largest portion of the total offset voltage except for resistive divider comparator [19]. After setting the widths of the mismatch critical transistors to have relatively large size (>1µm), the rest sizes of transistors are optimized for high speed, low offset and less power consumption.

Table1: Simulated Values With The Different Load Capacitance Of 7ff And 10ff For Selected Multi-Stage Dynamic Comparators

Design type	No. of transistors	∑ Width(µm)	Delay in ns When C=7fF	Delay in ns When C=10fF
Comparator1	10	18.4	0.29	0.46
Comparator2	11	18.4	0.198	0.31
Comparator3	14	18.4	0.116	0.18
Comparator4	15	18.3	0.098	0.15

VI. CONCLUSION

A new dynamic latched comparator which shows less sensitive in delay and higher load drivability than the conventional dynamic latched comparators has been designed. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented. As a result, the circuit shows up to 62% less sensitivity of the delay which is of about 0.098nsec than the conventional double-tail latched comparators at approximately the same area and power consumption.

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