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Efficient CAM based Low Power Analysis from Parity Check Method

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Abstract:- A Content Addressable Memory (CAM) is a Static RAM-based memory that can be accessed in parallel to search for a given search word, providing as a result the address of the matching data. This paper presents a new technique to reduce static and dynamic power consumption, increases speed in Content Addressable Memory (CAM).Our approach is to check most significant bits of CAM for search operation by breaking the match lines into several segments based on most significant bits. Since most stored words fail to match in their respective segments, the search operation is discontinued for corresponding segments. The technique proposed memory partition scheme by validating operating segments of CAM where the ideal portion should be short of to cut-off region using clock gating.

Keywords:- Content addressable memory (CAM), most significant bit, multiple input signature register, memory partition, clock gating.

I. INTRODUCTION

Content-addressable memory (CAM) is a special type of computer memory used in certain very high speed searching applications. It is also known as associative memory, associative storage or associative array, although the last term is more often used for a programming data structure. Several custom computers, like the Goodyear STARAN, were built to implement CAM, and were designated associative computers. CAM is a type of solid state memory in which data are accessed by their contents rather than physical locations. Content addressable memory (CAM) is an extension of RAM , we have to known the RAM features to understand CAM. IN General RAM has two operations read and write i.e. the data stored in RAM can be read or written. CAM has three operation modes: READ, WRITE, and COMPARE [1]. CAM are faster than other hardware and software based search systems.

Most memory devices store and retrieve data by addressing specific memory locations. The time required to find the data stored in memory can be reduced, if the data can be identified for access by its content rather than by its address. A memory that is accessed in this way is called content addressable memory(CAM). To achieve an effective function of data searching, the data comparisons architecture of CAM is usually implemented in parallel operation structure. The CAM has a parallel active circuitry which consumes more power and the main challenge in designing the CAM is to reduce the power consumption without reducing the speed and memory density.

CAM consisting of 4 words ,with each word containing 3 bits arranged horizontally.CAM search operation begins with loading the search data word into the search data registers followed by precharging all match lines high, putting them all temporarily match state. Next, the search lines drivers broadcast the search word onto the differential search lines, and each CAM core cell compares its stored bit against the bit on its corresponding search lines. Match lines on which all bits match remain in the precharged high state. Match lines that have atleast one bit that misses, discharge to ground. The MLSA then detects whether its match line has a matching condition or miss condition. Finally, the encoder maps the match line of the matching location to its encoded address [1].

Simple schematic CAM shows fig 1 the structure.CAM is used in application where search time is critical and very short. Basically CAM is used to design network routers for fast transfer or forwarding of packets. It is well suited for several functions like Ethernet address lookup, data compression, and security or encryption information on a packet –by-packet basis for high performance data switches.

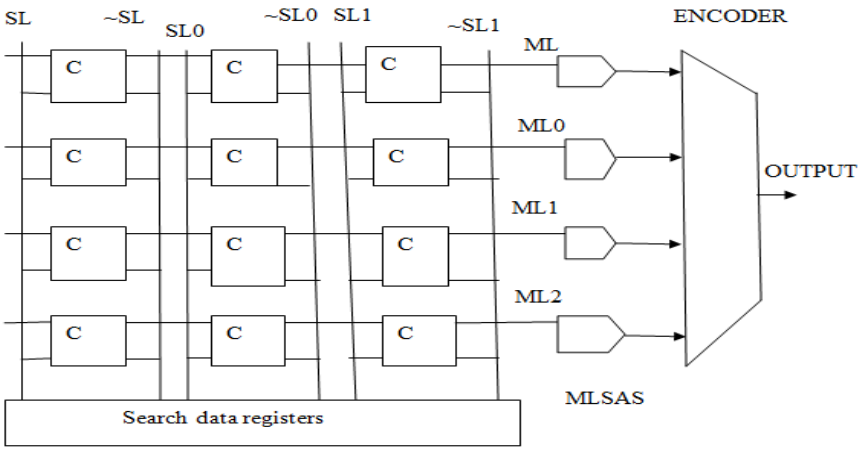

Fig.1: simple schematic of CAM

II. PROPOSED CAM

Parity bit is introduced to boost the search speed of the parallel CAM with less 1% power and area overhead and power consumption. In this proposed CAM is partitioned into two ways using parity bit.
The main objective of proposed CAM is to reduce power and increase speed of the CAM by using memory partition and clock gating. First we briefly discuss the conventional parity based CAM before presenting our proposed CAM.

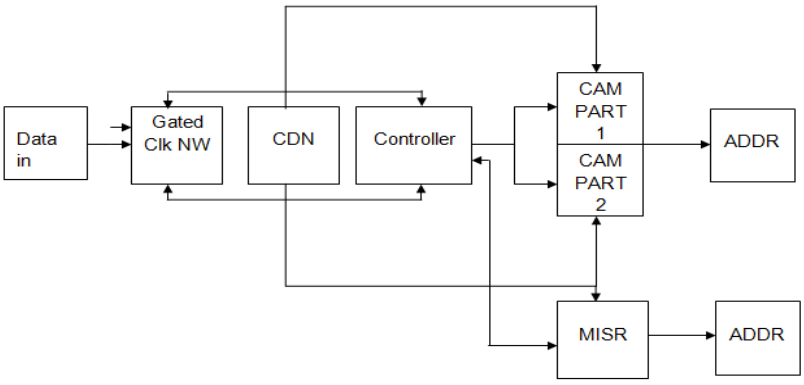

Fig.2: Block diagram of proposed CAM

A. Conventional Parity Bit Based CAM:

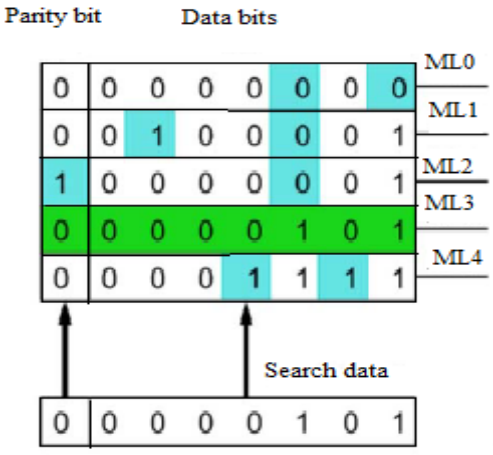

Fig.3: Conventional parity based CAM

The parity bit based CAM design is shown in Fig.2 consisting of the original data segment and an extra one-bit segment, derived from the actual data bits. These parity bit obtain i.e., odd or even number of "1"s. The obtained parity bit is placed directly to the corresponding word and ML [2]. The CAM using parity bit search the data using 0 or 1.we have to add the parity bit for every data bit, power consumes more. The effective gated power .The main drawback of the conventional CAM is transistor level power gating increases leakage current leads to chip violation. For highly recurrent input, CAM insists of searching address in whole memory based parity leads to latency reduction and throughput.

A. Proposed Parity bit CAM USING Memory Partition :

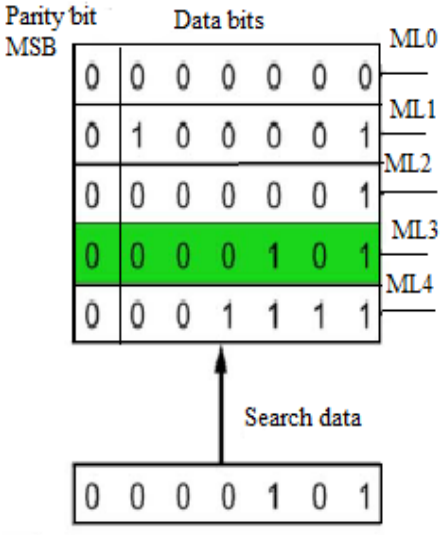

Fig .4: parity bit CAM using Memory partition

The proposed CAM design used to increase speed, reduce static and dynamic power consumption in content addressable memory (CAM) using memory partition and clock gating. Multiple input signature register is proposed to increase the searching speed of CAM by isolate recurrent data into signature memory, it reduces searching time. Our approach is to check most significant bits of CAM for search operation by breaking the match lines into several segments based on most significant bit. It increases speed and reduces power. Memory partition scheme by validating operating segments of CAM where the ideal portion should be using clock gating.

III. CLOCK GATING

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to the clock tree. Switching states consumes more power .This clock gating process can also save significant area as well as power. Clock gating uses to Register transfer level reduces power consumption. The main advantage of the clock gating sets the ideal mode when CAM is not in use in any other applications.

IV. PERFORMANCE COMPARISONS

Performance comparisons mainly discuss about flow summary and power play power analyzer using Quartus II and simulation using model sim 9.a.

A. Flow Summary of Proposed CAM:

Flow Status	Successful - Sun Mar 02 12:37:00 2014
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	CAM
Top-level Entity Name	CAM
Family	Cyclone II
Met timing requirements	Yes
Total logic elements	5 / 4,608 (< 1 %)
Total combinational functions	5 / 4,608 (< 1 %)
Dedicated logic registers	4 / 4,608 (< 1 %)
Total registers	4
Total pins	22 / 89 (25 %)
Total virtual pins	0
Total memory bits	2,048 / 119,808 (2 %)
Embedded Multiplier 9-bit elements	0 / 26 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP2C5T144C6
Timing Models	Final

Fig .5: Flow summary

This flow summary shows the area, total logic elements is less than 1% area using cyclone II family. This figure discuss about area and speed of CAM.

B. Power Play Power Analyzer Tool:

The power play analyzer tool discuss about static and dynamic power consumption of the CAM. In this total power dissipation values get through Quartus II. Dynamic power dissipation value is 2.61mW and static power dissipation is 18.04mW. Finally, the total power dissipation is 46.30 mW.

PowerPlay Power Analyzer Status	Successful - Sun Mar 02 12:39:42 2014
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	CAM
Top-level Entity Name	CAM
Family	Cyclone II
Device	EP2C5T144C6
Power Models	Final
Total Thermal Power Dissipation	46.30 mW
Core Dynamic Thermal Power Dissipation	2.61 mW
Core Static Thermal Power Dissipation	18.04 mW
I/O Thermal Power Dissipation	25.64 mW
Power Estimation Confidence	Medium: user provided moderately complete toggle rate data

Fig.6: power play power analyser tool

C. RTL Schematic View:

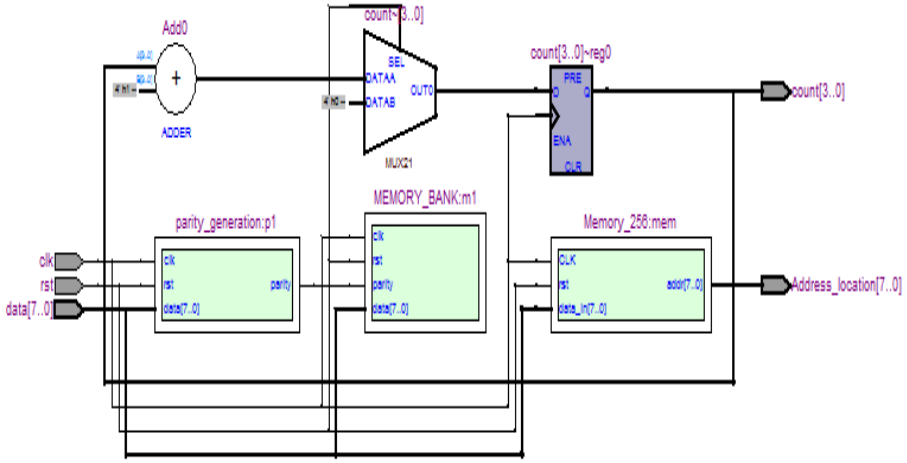

Fig.7: RTL schematic view

D. Simulation :

The figure 8 and figure 9 shows the existing and proposed CAM.

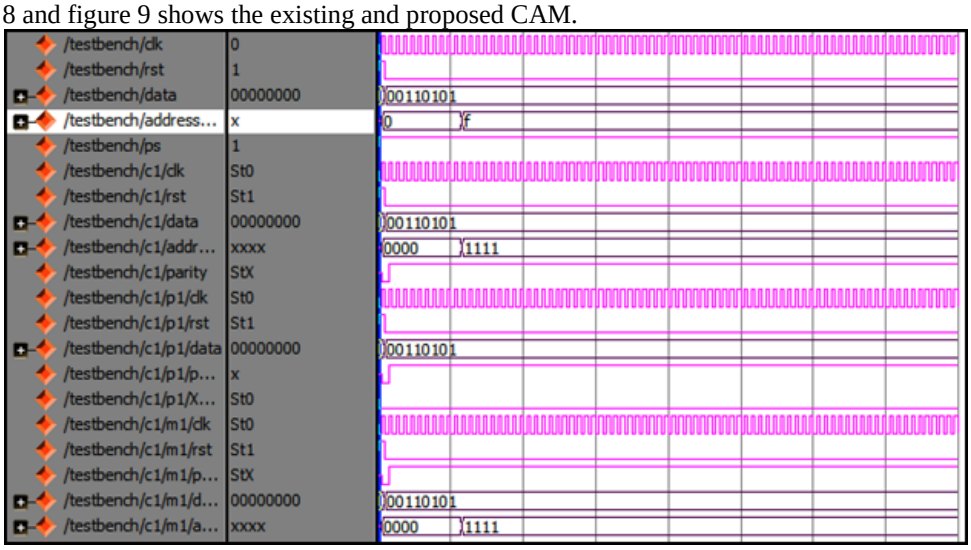

Fig. 8: simulation of existing CAM

In this fig 8 shows the existing system of CAM having more parity generation, it consumes more power.

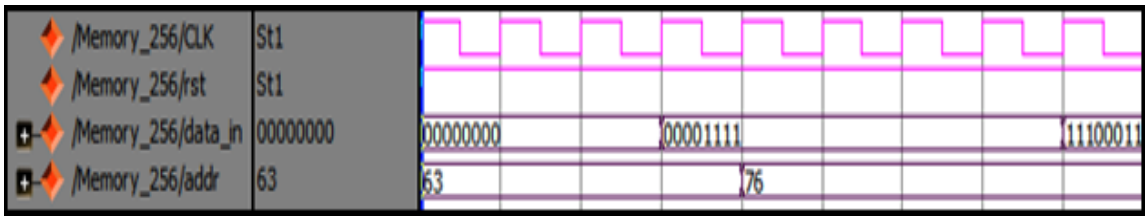

Fig. 9: simulation of proposed CAM

In this fig 9 shows the simulation of proposed CAM having less number of parity generation using memory partition ,it reduces area and increases speed.

E. Comparison Table:

The table 1 shows the existing system and proposed system of CAM

Table I: Comparison Table

Method	Total Logic Elements	Static Power Dissipation	Dynamic Power Dissipation	Total Power Dissipation
Existing System	325/14.448(2%)	47.91mw	78.09mw	369.90mw
Proposed System	5/4.608(1%)	18.04mw	2.61mw	46.30mw

F. Bar diagram:

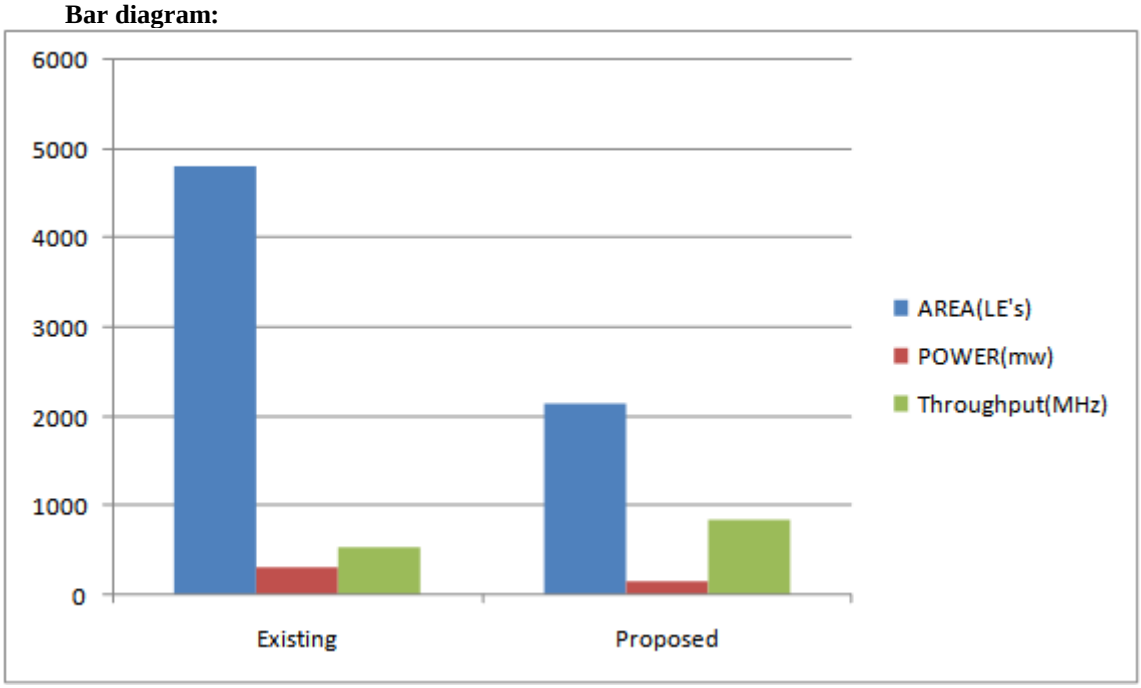

Fig.10: Bar diagram of existing and proposed CAM

V. CONCLUSIONS

We proposed an effective clock gating technique and a memory partition that offers several major advantages, namely average power consumption, boosted search speed and improved process variation. It is much more stable than recently published designs while maintain their low power consumption. The proposed CAM is well suitable for sub-65-nm CMOS technology.

In future CAM can be used to accelerate any application ranging from Local area network, data base management and file storage management.

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