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IC Interconnects Modeling using X-parameters

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Abstract:-The performance of IC interconnects has been stretched tremendously recently years by high speed integrated circuit systems. Even though S-parameters are popularly used for the characterization of IC interconnects, their modeling has to consider the existence of active devices, such as buffers and drivers. The I/O model is difficult to obtain due to the IP protection and limited information. In this paper, we propose to use the X-parameter to model the IC interconnect system. Based on the PHD formalism, X-parameter models provide an accurate frequency-domain method under large-signal operating points to characterize their nonlinear behaviors. Another challenge is that in the digital IC system, the digital signal is best represented in the time domain while S-parameter and X-parameter are both in the frequency domain. Hence, a proper control of the harmonic contents inside the input signal to drivers and buffers are needed. Starting from modeling the CMOS inverter, we present the whole link modeling primarily based on X-parameter for the pulsed digital signal. According to our knowledge, this is the first time X-parameter is applied for this type of applications.

Keywords:-Buffer; nonlinearity; polyharmonic distortion; digital pulse signal; X-parameters.

I. INTRODUCTION

Over past decades, the signal speed of modern integrated circuits (IC) has spiked to gigahertz level. Consequently, the working bandwidth is significantly expanded. Unlike analog amplifiers, buffers and drivers, implemented by the CMOS technology, work under the extreme nonlinear mode. They show strong pull-up and push-down IO behaviors. Therefore, the famous IBIS model is able to become a popular facility to serve as the behavior model of the IC IOs. However, IBIS models are based on the I-V curve measurements. They lack the parasitic coupling information and are found that it does not work well for high speed signals in the digital system.

For the high speed system, the network parameter S-parameter is used to characterize the frequency response of passive parasitic structures, such as IC interconnects, packaging, etc. However, it is not good for digital devices because S-parameter is only good for linear devices. Devices in IC circuits, such as buffers or drivers, demonstrate extreme nonlinearity. To accurately model digital devices, one way is to use the accurate SPICE model. However, it is not trivial to obtain the SPICE model, especially when the working frequency is high. Meanwhile, it is preferred in industries to maintain the IP privacy as much as possible. Hence, this makes it even more difficult to find the proper SPICE model of the device. The behavior model is not considered to be intrinsic because it involves too many approximations. A better nonlinear device modeling technique is needed.

X-parameter is a new technology developed by Root and Wood [1] for the characterization of nonlinear devices. Mathematically S-parameter can be considered as the special linear case of X-parameter. It was first introduced from the polyharmonic distortion (PHD) modeling [2, 3]. It is not only suitable to existing nonlinear simulation methods, but also can be measured through commercial nonlinear vector network analyzers. It makes the conventional linear black box into the nonlinear black box. It has been applied for analog devices in communication systems. However, there are very limited trials for using X-parameter technologies in the digital circuits. Its practical trial for the signal integrity analysis is rare. In [4], the X-parameter was first experimented for the high speed link I/O modeling. However, it uses the sinusoidal signal as the input signal that is very different from digital signals being used in practical IC system. However, it is not trivial to add a DC pulse sequence signal into the input of X-parameter simulation link because the spectrum of the input signal will be much more complicated than the sinusoidal one. However, to analyze the cross talk and noise coupling mechanism, it is necessary to apply the real digital signal into the system. From [5], X-parameter models showed a great agreement with analog LNA with pulse input signals for the first time. We continue to advance the work to investigate the X-parameter behaviors.

In this paper, we propose to use the real digital pulse signal to excite the high-speed I/O link modeled by X-parameters. The impacts of harmonic truncations to the nonlinear behavior characterization will be carefully discussed. The power exponential pulse signal is also applied to observe its response through digital devices modeled by X-parameters. A complete IO link is benchmarked with X-parameters in the end of this paper. According to what we have read, this is the first time X-parameter is used for the true IC interconnect modeling with realistic digital signal inputs. Therefore, it provides the first look at the performance of X-parameters for IC signal integrity modelling.

The remainder of this paper is organized as follows. The PHD models represented along with X-parameters are introduced first. Next, the methodologies of building X-parameter models and processing pulse signals for X-parameter simulations are presented. Then, simulation studies using the representative digital CMOS inverter and buffer for IC interconnect link are given and discussed to demonstrate the performance of X-parameter models for pulse signals in signal integrity.

II. PHD AND X-PARAMETER FORMULATIONS

The basic concept of X-parameters is proposed on the PHD model, which is based on the principle of harmonic superposition and the nonanalytic property of the spectrum mapping function of the nonlinear system. It can be treated as the nonlinear extension of the linear S-parameter [2]. It intends to implement a frequency domain black box modeling approach. Assume the nonlinear circuit has N signal ports. The incident wave with the frequency harmonic index l at port q can be defined as A_{ql} while the scattered wave with the frequency harmonic index k at port p can be defined as B_{pk}. Then the spectrum mapping function of the nonlinear system from all input frequency contents of all signal ports to the single scattered wave at the signal port p with the frequency k is.

$$\boldsymbol{B_{pk} = F_{pk}(A_{11}, A_{12}, \dots, A_{21}, A_{22}, \dots, A_{N1}, A_{N2}, \dots)} \quad \textbf{(1)}$$

Then the A-wave can be defined using S-parameter type concept as

$$\boldsymbol{A_{ql} = \frac{V_{ql} + Z_{cql} I_{ql}}{2}} \quad \textbf{(2)}$$

$$\boldsymbol{B_{pk} = \frac{V_{pk} + Z_{cpk} I_{pk}}{2}} \quad \textbf{(3)}$$

Then based on the harmonic superposition, the scattered B wave can be generally represented by A_{11}, A_{ql} and the conjugate of A_{ql}:

$$\begin{aligned}\boldsymbol{B_{pk}(|A_{11}, f|)} &= \boldsymbol{X_{pk}^{(FB)}(|A_{11}, f|) \cdot P^{k}} \\ &\quad + \sum_{q=1}^{q=N} \sum_{l=1}^{l=M} \boldsymbol{X_{pq,kl}^{(S)}(|A_{11}, f|) \cdot P^{k-l} \cdot A_{ql}} \\ &\quad + \sum_{q=1}^{q=N} \sum_{l=1}^{l=M} \boldsymbol{X_{pq,kl}^{(T)}(|A_{11}, f|) \cdot P^{k+l} \cdot A_{ql}^{*}}\end{aligned} \quad \textbf{(4)}$$

Because the phase term is only referred to the fundamental frequency,

$$\boldsymbol{X_{p1,k1}^{(S,T)} = 0} \quad \textbf{(5)}$$

In above formulation, P is the phase term of the fundamental frequency.

$$\boldsymbol{P = e^{jArg(A_{11})}} \quad \textbf{(6)}$$

$X_{pq,kl}^{(S)}$ is a scattering parameter that accounts for the contribution to the k^{th} harmonic at port p due to the l^{th} harmonic of the incident wave in port q. It is very much similar to the conventional concept of S-parameter except that it supports the relationship between different harmonic frequencies. $X_{pq,kl}^{(T)}$ is a new type of scattering parameter that accounts for the contribution to the k^{th} harmonic at port p due to the l^{th} harmonic of the conjugated incident wave in port q. It is very unique to PHD method. It accounts the impact of the phase from high order harmonic inputs. In (6), P is a pure phase along with the magnitude-only dependence on A_{11} by convention [2]. The S and T functions describe a full set of parameters to completely characterize the nonlinearities.

III. X-PARAMETER MODELING FOR IC INTERCONNECTS

In this paper, we employ Agilent ADS [6] to implement the X-parameter modeling of IC interconnects,which is partitioned into two parts: passive interconnects and active devices. Since the passive part is linear, conventional S-parameter can be utilized for its characterization. However, active devices such as buffers in the system are of strong linearity. Hence, X-parameter will be used to model them. To illustrate the proposed method clearly, we exclusively use ADS in this paper, including the X-parameter extraction of the device.

A. Input Signals

The first step is to extract the X-parameter of the device. It is convenient to extract the X-parameter model from a given SPICE model of the device in ADS. However, one issue is critical: what are the fundamental frequency and its harmonics? It is related to the setup of M in equation (4).

If the input signal is sinusoidal, the input setup is trivial. However, if the input is a practical periodic pulsed digital signal as shown in the left figure of Fig. 1, there are many spectrum contents being input into the device and thereby the X-parameter model during its application. An example of the rich spectrum content is shown in the right figure of Fig. 1. It shall be noted that there is a very strong DC component in the spectrum due to the fact that the given pulse signal swings between 0 Volt and 5 Volt in this example.

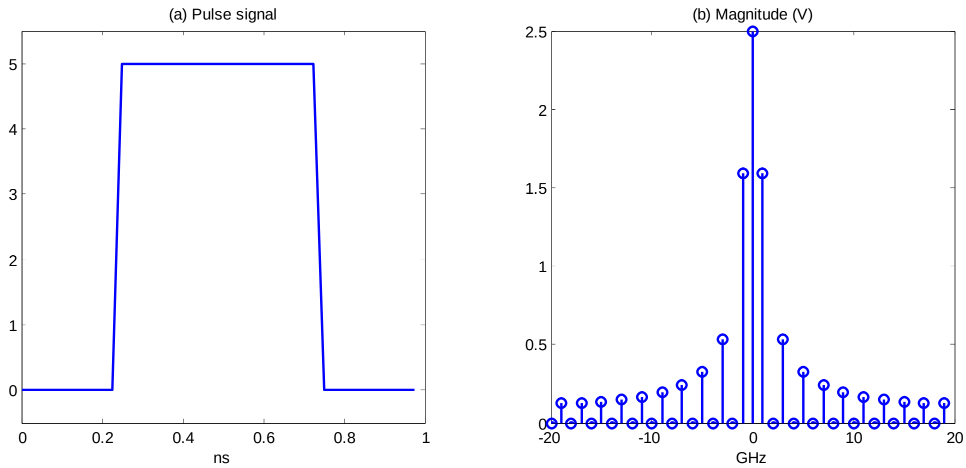

Fig. 1:Input pulse signal in (a) the time domain and (b) the frequency domain.

If the pulse signal has zero rise and fall times, the wide of the signal is τ and the period of the pulse sequence is T, its Fourier series expansion is

$$\boldsymbol{s(t) = v_0 \frac{\tau}{T} + v_0 \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{\pi n \tau}{T}\right) \cos\left(\frac{2\pi n}{T} t\right)} \qquad \textbf{(7)}$$

Obviously the spectrum contents are discrete with a DC term that is directly determined by the space ration of the pulse signal. All spectrum contents are in the harmonic position of $\omega_0=2\pi/T$. For digital circuits, every bit contains the same width. Therefore, $\tau = 0.5T$. Equation 7 becomes

$$\boldsymbol{f(t) = \frac{\tau}{T} + \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{\pi}{2} n\right) \cos(\omega_0 n t) = \frac{\tau}{T} + \sum_{m=0}^{\infty} \frac{2}{(2m+1)\pi} (-1)^m \cos\big((2m+1)\omega_0 t\big)} \qquad \textbf{(8)}$$

Several important features can be obtained from the above equation. First, the spectrum contents only have odd harmonics of the fundamental frequency. Even harmonics are all zeros. Meanwhile, the magnitude of all harmonics is inversely proportional to its order number. If we check the first 4 nonzero harmonics starting from the fundamental one, the magnitudes are

$$\boldsymbol{\frac{2}{\pi}, \frac{2}{3\pi}, \frac{2}{5\pi}, \frac{2}{7\pi}, \dots}$$

Apparently the fundamental frequency is significantly larger than all other high order harmonics. This satisfies the critical preliminary requirement that the harmonic superposition is being used by the X-parameter. Hence, it works to use X-parameter to model the pulsed input signal in the IC interconnect.

Because the number of harmonics could be infinite, another question is how to decide its truncation number. There comes the knee frequency in the CMOS technology. In reality, the pulsed signals in the digital signal can only have nonzero rise time. By calculating its spectrum, it can be seen that after certain frequency, the signal power of the digital signal spectrum begins to drop dramatically faster than 20 dB/decade. This turning point is defined as the knee frequency. It is a proper frequency above which spectrum in the signal spectrum can be ignored without causing many errors in most analyses.

If the 10% to 90% rising time of the digital signal is defined as $t_{10\text{-}90}$, the empirical equation of the knee frequency is

$$f_{knee} = \frac{0.35}{t_{10-90}} \tag{9}$$

Because today's digital signals require to transmit data at multi-gigabit rates, the rise time is assumed to be the nano or pico second scale. The faster the rise time is, the higher the knee frequency is. Hence, more significant high frequency terms need to be preserved. If we assume the rise time of the pulse signal in Fig. 8 is 25 ps, the knee frequency is about 14 GHz. Hence, it is necessary to employ 14 harmonics to represent the pulse signal propagating in the IC interconnect system.

B. X-Parameter Extraction and Simulation

With the known information of input signals, the X-parameter models of the device can be extracted accordingly. Agilent ADS can be used to obtain X-parameters if the device SPICE model is available.

It has to be noted that the X-parameter model in ADS only accepts power input sources. Hence, the pulse signal being used for digital IC interconnects cannot be directly used for the X-parameter extraction. To solve this issue, the Fourier transform is applied on the periodic pulse signal first. Using the harmonic truncation principle mentioned in the previous section, a sequence of power input sources based on the spectral components of the pulse signal is selected and composed. Then they are treated as the X-parameter generation source, which is corresponding A_{ql} in equation 4.

The generated X-parameter model is then used in the harmonic balance simulation process for nonlinear circuits. The harmonic contents of input pulsed signals are employed again. It is critical to know that not only the magnitude but also the phase of each harmonic is needed in both X-parameter extraction and the harmonic balance simulation.

The output of the nonlinear simulation is a series of harmonic spectrum components. Inverse Fourier transform is utilized to recover the time domain waveform.The schematic of one of the examples for the X-parameter model generation is demonstrated in Fig. 2. This process is graphically shown in Fig. 3.

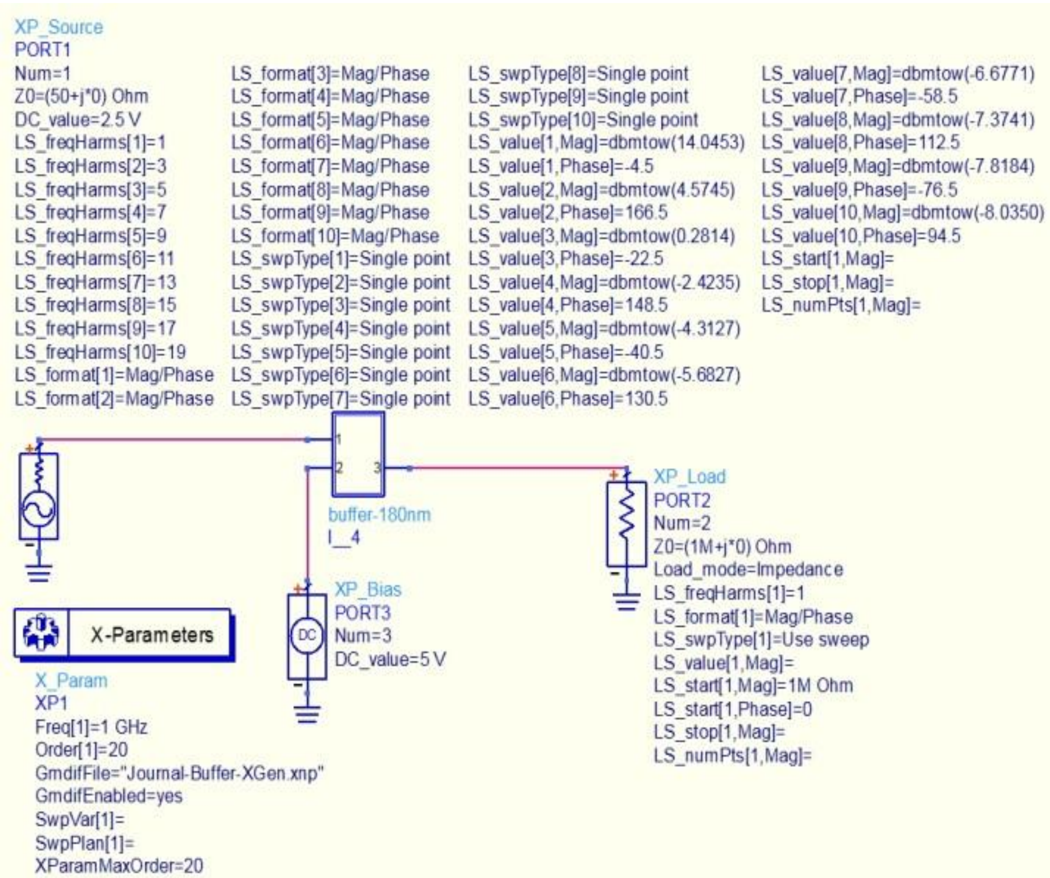

Fig. 2: The schematic of the X-parameter generation setup in ADS.

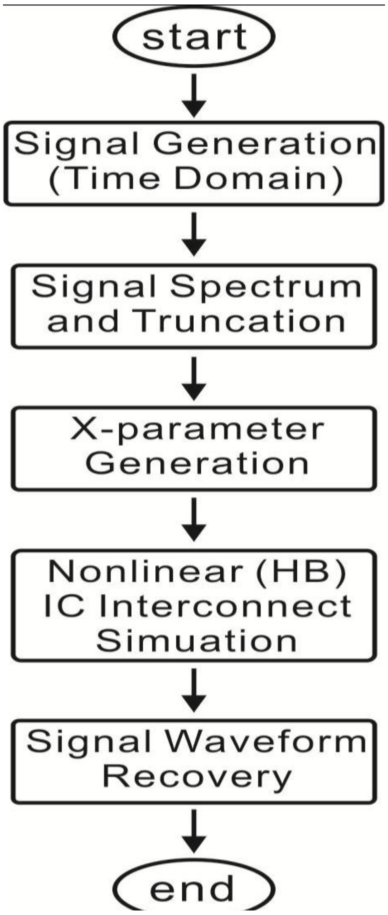

Fig. 3: The X-parameter simulation process for pulse signals.

C. CMOS Inverter and Buffer

The CMOS technology is popularly used in today's IC devices. The CMOS inverter is the most fundamental device. In this paper, we employ the 0.18 µm technology to construct the inverter. Later it will be used to build the CMOS buffer. To validate the inverter, 1-GHz fundamental frequency in the Harmonic Balance simulator was implemented.

The generation of the X-parameter model for the CMOS inverter follows the same procedure as described previously. The input pulse signal and its spectral components are shown in Fig. 1 for both time and frequency domains. The pulse signal is designed to have a 5-Volt amplitude. The average magnitude DC point is observed at 2.5 voltages.

If the fundamental frequency is 1-GHz, different number of harmonics inputted into the X-parameter model of the inverter will generate different output. After recovering the time domain wave form, it becomes obvious that more input harmonics will generate better output waveform. Meanwhile, if the harmonic balance simulation is applied on the inverter's SPICE model directly, the output can be employed as the reference. Fig. 4 depicts the output from X-parameter model using 1, 5, 10, and 20 input harmonics for the inverter and their comparisons with the direct SPICE model simulation result (in Green dash lines). It is observed that within the number of truncated harmonic numbers, the X-parameter model can generate the same output as that of the SPICE model. With increasing number of harmonics, the waveform migrates gradually to a smoother waveform in the time domain to reduce the Gibbs phenomena.

The CMOS buffer is composed of a couple of identical CMOS inverters. Using the 0.8 µm CMOS technology mentioned before, a buffer can be easily constructed in the simulator. A 1-GHz large signal was first used to excite the CMOS buffer at the fundamental frequency. Small signal tones are then sent to the input port at the harmonic frequencies of the fundamental. Next, the output waveforms of the buffer with 5, 10, 14, and 20 harmonic inputs given in Fig. 5 illustrate the comparison with the direct buffer model.

Fig. 5 shows the DC and different selected harmonic numbers results of the buffer. When the number of harmonics rises, the error of approximation is reduced accordingly. With 14 harmonics, the error is very similar to the case with 20 harmonics. This implies the knee frequency is a proper option for truncation selection. Also, a convergence to a fixed height is also observed in the last two plots of Fig. 5.

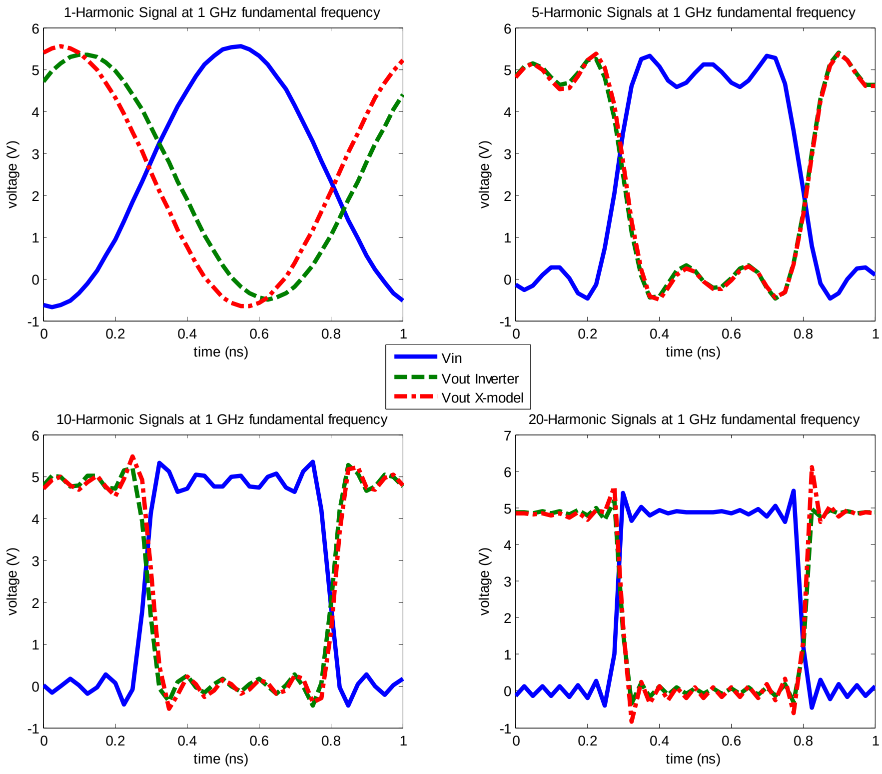

Fig. 4:DC + 1, 5, 10, and 20 Harmonic signals of CMOS inverter with 1 GHz fundamental frequency.

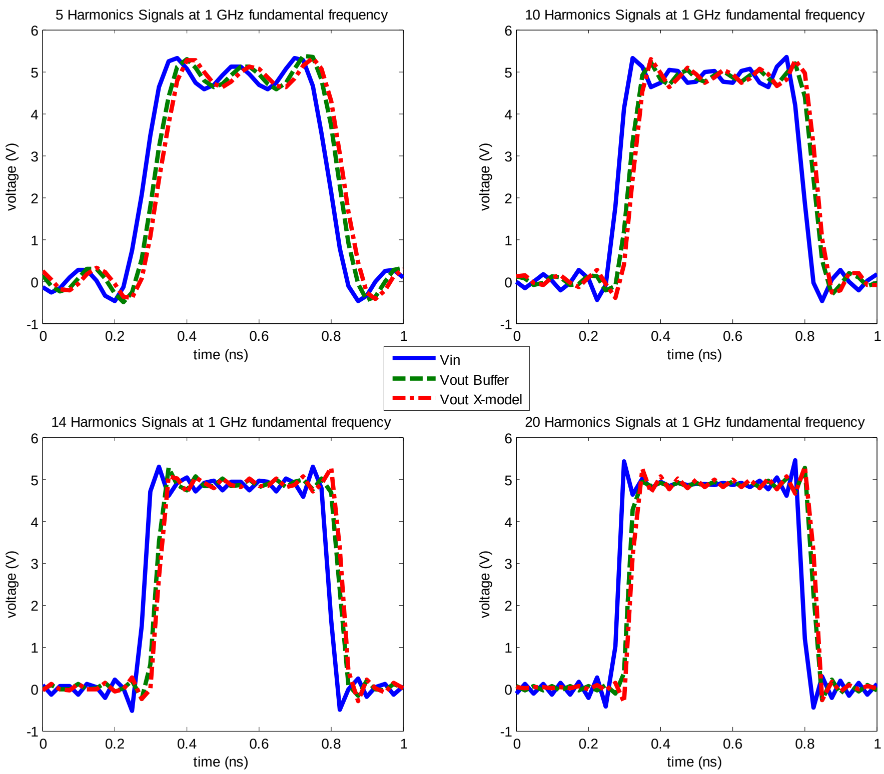

Fig. 5:DC + 5, 10, 14, and 20 Harmonic signals of CMOS buffer with 1 GHz fundamental frequency.

D. Transmission line with Buffer

Next, we can cascade the buffers together with transmission lines to form a complete IC interconnect link. The harmonic balance is used as the simulation method. The buffers are represented by the X-parameter. The transmission lines are modeled by the transmission line model. Fig. 6 shows the two buffers cascaded with a transmission line in-between. We want to test the buffer's functionality along with the near and far end crosstalk on the other transmission line. The results of using the direct solver and X-parameter models are shown in Fig. 7 (a), and a significant delay is observed on the voltage output between them. This delay is due to a systematic issue in ADS. It uses the interpolation to generate output spectrum from X-parameter blocks in ADS. Although the input spectrum of first stage is exactly the same with it in xnp generation,the output spectrum is changed. Therefore, with single point xnp, the output of second stage may have several degree phase differences compared to real circuit. With more stages of cascade, the phase error is also increased [7]. In this case, because there is only one input data of original xnp, ADS does not have much information for interpolation. This causes the phase error.

In order to reduce the delay, another way we tried is to use the whole subcircuit as one X-parameter model. The other validation uses the whole setup shown in Fig. 6 all together as one X-parameter model. This reduces the flexibility of X-parameter usage since this X-parameter can be only used for this circuit or structure on purpose. The voltage output of direct solver and X-parameter model are shown in Fig. 7 (b). Clearly we see no time difference issue except a small glitch on the edge for the X-parameter model. As a result, there is a phase interpolation error in the ADS simulation.

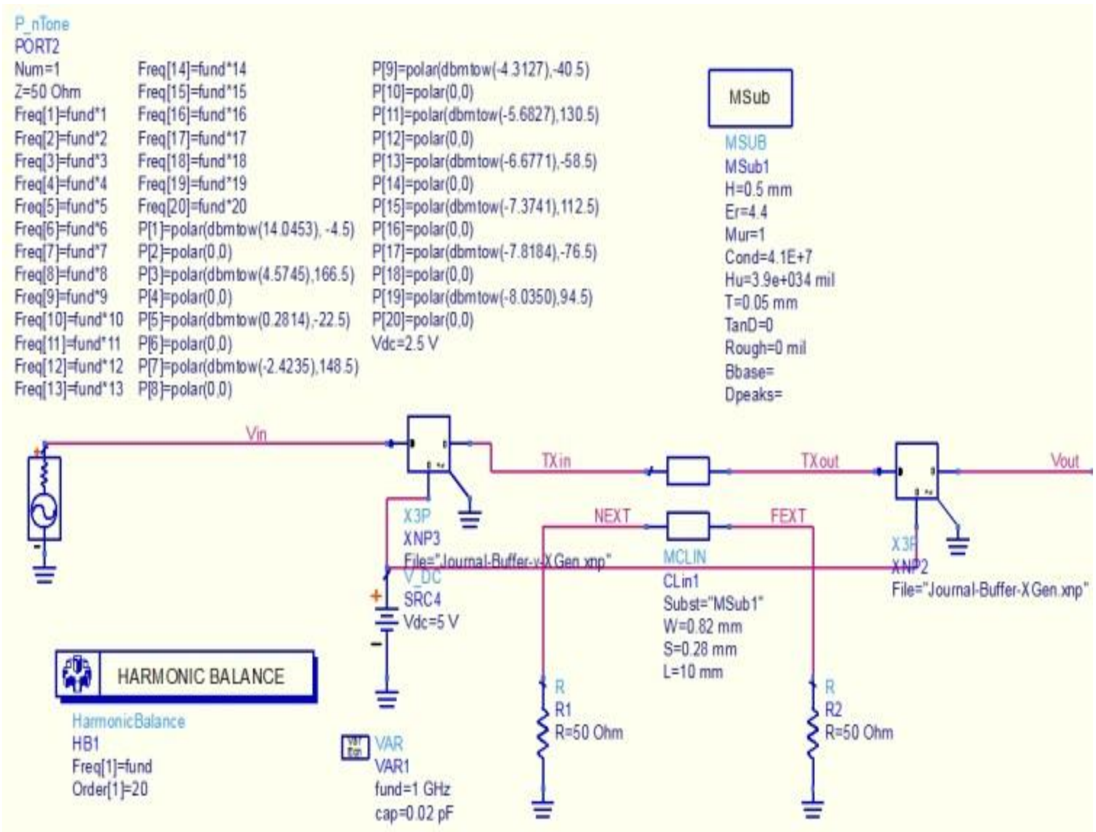

Fig. 6:The schematic of the transmission line with buffers in ADS.

IV. CONCLUSIONS

In this paper, the digital pulse signal response of IC interconnectsismodeled and simulated using X-parameter models. It is the first complete trial of the X-parameter to IC interconnects signal integrity analysis. The benchmarks demonstrated that X-parameters/PHD formulations with the proper truncation of harmonics can produce satisfactory results. Compared to direct solving, the X-parameter models can obtain great agreement in the simulated data regarding to the nonlinear property of digital circuits. Overall, the potential of X-parameters can be further explored for its extensive applications for signal integrity issues in IC interconnect and packaging modelling.

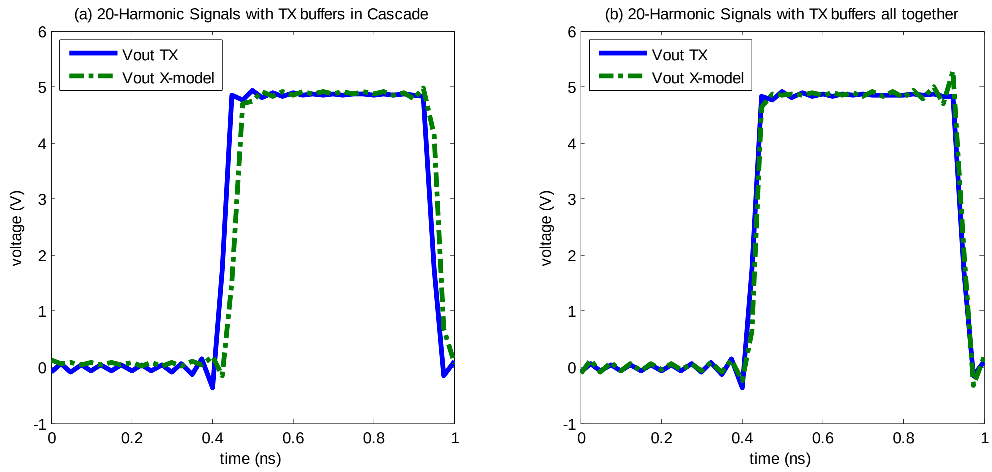

Fig. 7:DC + 20 Harmonic signals of CMOS buffers with transmission line at 1 GHz fundamental frequency. (a) X-parameters models in cascade. (b) Circuits all together as one X-parameter model.

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