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AC/DC Converter with Active Power Factor Correction Applied to DC Motor Drive

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Abstract*—Harmonic pollution and low power factor in power systems caused by power converters have been of great concern. To overcome these problems several converter topologies using advanced semiconductor devices and control schemes have been proposed. This investigation is to identify a low cost, small size, efficient and reliable ac to dc converter to meet the input performance index of UPS. The performance of single phase and three phase ac to dc converter along with various control techniques are studied and compared. This paper presents a novel ac/dc converter based on a quasi-active power factor correction (PFC) scheme. In the proposed circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc fly back converter. The auxiliary winding is placed between the input rectifier and the low-frequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since the dc/dc converter is operated at high-switching frequency, the auxiliary windings produce a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. It eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher efficiency. Finally a DC motor load is applied and simulation results are presented.*

Index Terms—AC/DC converter, power factor correction, single stage**.**

I. INTRODUCTION

Switched mode Power Factor Corrected (PFC) AC-DC converters with high efficiency and power density are being used as front end rectifiers for a variety of applications [1-3]. The converters are either buck or boost type topologies. The buck type topology provides variable output DC voltage, which is much lower than the input voltage amplitude. However when the instantaneous input voltage is below the output DC voltage, the current drops to zero that results in significant increase in input current THD. Even with input filters the buck converters provide only limited improvement in input current quality. On the other hand the boost type converter always produces the output voltage higher than the input instantaneous voltage amplitude. The boost inductor with appropriate choice helps to maintain continuous input current with good wave shape. This lead the converter control to maintain near unity power factor, low input current THD and good output voltage regulation.

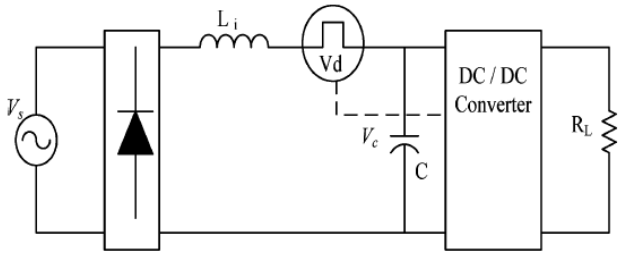


Fig.1: General circuit diagram of rectifier with PFC cell.

Two-stage scheme results in high power factor and fast response output voltage by using two independent controllers and optimized power stages. The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications. In order to reduce the cost, the single-stage approach, which integrates the PFC stage with a dc/dc converter into one stage, is developed [1]–[11]. These integrated single-stage power factor correction (PFC) converters usually use a boost converter to achieve PFC with discontinuous current mode (DCM) operation. Usually, the DCM operation gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode (CCM). However, the CCM operation yields slightly higher efficiency compared to the DCM operation. A detailed review of the single stage PFC converters is presented in [3]. Generally, single-stage PFC converters meet the regulatory requirements regarding the input current harmonics, but they do not improve the power factor and reduce the THD as much as their conventional two-stage counterpart. To overcome the disadvantages of the single-stage scheme, many converters with input current shaping have been presented [3]–[12], in which a high frequency ac voltage source (dither signal) is connected in series with the rectified input voltage in order to shape the input current (see Fig:1). In this paper, a new technique of quasi-active PFC is proposed. As shown in Fig. 2, the PFC cell is formed by connecting the energy buffer (*LB*) and an auxiliary winding (*L*3) coupled to the transformer of the

dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced.

II. PROPOSED QUASI-ACTIVE PFC CIRCUIT

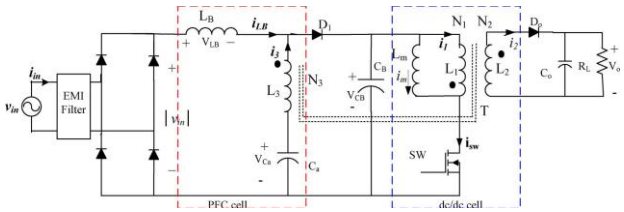


Fig. 2. Proposed Quasi Active PFC Circuit Diagram

Flyback Converter Topology

Fly-back converter is an isolation converter. Its topology is shown in Fig.3(a).Fig 3(b) shows its input current waveform. The input voltage-input current relationship is similar to that of buck-boost converter.

$$I_{avg}(t) = (D^2Ts/2L_m)\, V_1(t) \qquad (1)$$

Where, L_m is magnetizing inductance of the output transformer

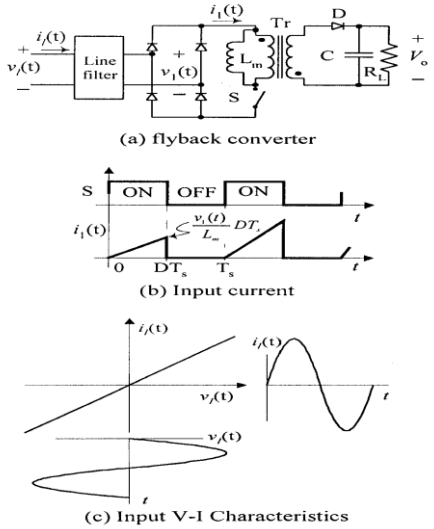


Fig.3.Basic Fly-back Converter

The proposed quasi-active PFC circuit is analyzed in this section. As shown in Fig. 2, the circuit comprised of a bridge rectifier, a boost inductor *LB*, a bulk capacitor *Ca* in series with the auxiliary windings L3 , an intermediate dc-bus voltage capacitor *CB* , and a discontinuous input current power load, such as fly back converter. The fly back transformer (*T*) has three windings *N*1,*N*2 , and *N*3 . The secondary winding *N*2 = 1is assumed. In the proposed PFC scheme, the dc/dc converter section offers a driving power with high-frequency pulsating source. The quasi active PFC cell can be considered one power stage but without an active switch.

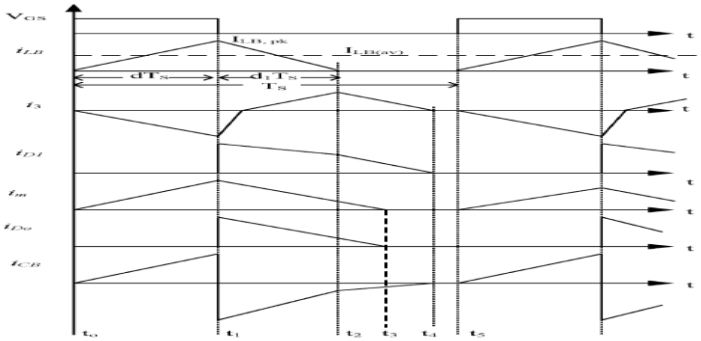


Fig.4. Key switching waveforms of the proposed PFC.

To facilitate the analysis of operation, Fig :5. shows the topological stages and the key waveforms of the proposed circuit. It is assumed that both the input inductor *LB* and the magnetizing inductance of the fly back converter operate in DCM. Therefore, currents *iLB*, *im*, and *i*2 are zero at the beginning of each switching period. It is also assumed that the average capacitor voltage *VCa* is greater than the average rectified input voltage |*v*in |. To ensure proper operation of the converter, the transformer's turns ratio should be (*N*1/*N*3) ≥ 2 and the boost inductor *LB* < *Lm*. In steady-state operation, the topology can be divided into four operating stages.

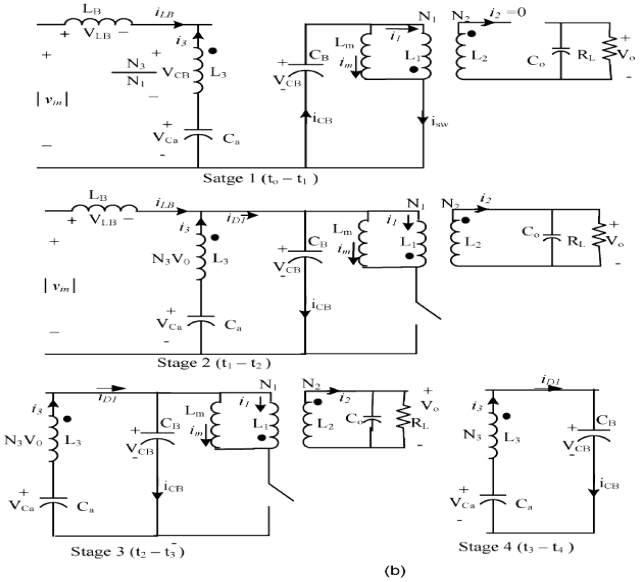


Fig.5. Equivalent circuit operation stages of the proposed PFC circuit during one switching period.

1) Stage 1 (to − t1): When the switch (SW) is turned on at *t* = *to* , diodes *D*1 and *Do* are OFF, therefore, the dc-bus voltage *VCB* is applied to the magnetizing inductor *Lm*, which causes the magnetizing current to linearly increases. This current can be expressed as

$$i_m = \frac{V_{CB}}{L_m}(t_o - t_1). \qquad (2)$$

And since diode *D*1 is OFF, the input inductor *LB* is charged by input voltage, therefore, the inductor current *iLB* is linearly increased from zero since it is assumed that the PFC cell operates in DCM. This current can be expressed as

$$i_{LB} = \frac{|V_{\text{in}}| + (N_3/N_1)V_{CB} - V_{Ca}}{L_B}(t_o - t_1) \qquad (3)$$

where, *V*in = *Vm*| sin *θ*| is the rectified input voltage, (*to* − *t*1) = *dTS* is the ON-time of the switch (SW), *LB* is the boost inductor and *N*1 , *N*3 are the primary and auxiliary turns ratio, respectively. At this stage, *iLB* = −*i*3 and the capacitor *Ca* is in the charging mode. On the other hand, *Do* is reversed biased and there is no current flow through the secondary winding.Since the transformer is assumed ideal, based on Ampere's law, it has

$$N_1 i_1 + N_2 i_2 - N_3 i_{LB} = 0$$

where $i_2 = 0$ at this stage therefore,

$$i_1 = \frac{N_3}{N_1} i_{LB} = -\frac{N_3}{N_1} i_3. \qquad (4)$$

Thus

$$i_m = i_{CB} - i_1 = i_{CB} + \frac{N_3}{N_1} i_3. \qquad (5)$$

Therefore, from (4) it can be seen that the magnetizing current *im* is supplied by the discharging current from the dc bus capacitor *CB* and the current *i*3 which is equal to input current *iLB* at this stage. The current through the main switch (SW) is given by

$$i_{\text{SW}} = i_{CB} = i_m - \frac{N_3}{N_1} i_3 = i_m + \frac{N_3}{N_1} i_{LB}. \qquad (6)$$

Therefore, the current stress of the switch can be reduced by selecting the turns ratio (N), which is designed to be less than 1 to ensure proper operation of the transformer. Compared to the single-stage BIFRED converter [11], the switch current is given by

$$i_{\mathrm{SW}} = i_m + i_{LB}. \quad \textbf{(7)}$$

Obviously, the proposed circuit has less switch current stress, LB therefore, the conduction loss and switching losses are reduced, and the efficiency is improved correspondingly. This stage ends when the switch is turned off at t = t1.

2) Stage 2 (t1 − t2): When the switch is turned OFF at $t = t1$, output diode *Do* begins to be forward biased. Therefore, the energy stored in the transformer magnetizing inductor is delivered to the load through the secondary winding. imilarly, the diode *D*1 is also forward biased and the voltage across *LB* now *V*in − *VCB*. Therefore, the current I is linearly decreased to zero at t = t2 LB (DCM operation), and the energy stored in L is delivered to the dc bus capacitor CB. Therefore

$$i_{LB} = \frac{|V_{\mathrm{in}}| - V_{CB}}{L_B}(t_1 - t_2). \quad \textbf{(8)}$$

The capacitor (Ca) is also discharging its energy to the dc bus capacitor CB and the current I reverse its direction. Therefore, the capacitor current is given by

$$i_{D_1} = i_{CB} = i_{LB} + i_3. \quad \textbf{(9)}$$

3) Stage 3 (t2 − t3): At this stage, the input inductor current *iLB* reaches zero and the capacitor *Ca* continues to discharge its energy to the dc bus capacitor *CB* . Therefore, *iD*1 = *iCB* = *i*3 . At $t = t3$, the magnetizing inductor releases all its energy to the load and the currents *im* and *i*2 reach to zero level because a DCM operation is assumed.

4) Stage 4 (t3 − t4): This stage starts when the currents *im* and *i*2 reach to zero. Diode*D*1 still forward biased, therefore, the capacitor *Ca* still releasing its energy to the dc bus capacitor *CB* . This stage ends when the capacitor *Ca* is completely discharged and current i3 reaches zer0. At t=t5. The switch is turned on again to repeat the switching cycle.

Steady-State Analysis:
The voltage conversion ratio of the proposed converter can be estimated from the volt-second balance on the inductors and the input–output power balance as explained in the following. From the volt-second balance on *LB*

$$\left(V_{\mathrm{in}} + \frac{N_3}{N_1}V_{CB} - V_{Ca}\right) dT_S = (V_{CB} - V_{\mathrm{in}})\, d_1 T_S \quad \textbf{(10)}$$

where *d*1 is the OFF-time of the switch (SW). Therefore, *d*1
could be given by

$$d_1 = \frac{V_{\mathrm{in}} + (N_3/N_1)\, V_{CB} - V_{Ca}}{V_{CB} - V_{\mathrm{in}}} d. \quad \textbf{(11)}$$

the average current of the boost inductor in a switching cycle is given by

$$I_{\mathrm{in}} = I_{LB,\mathrm{av}} = \frac{i_{LB,\mathrm{peak}}}{2}(d + d_1)\, T_S. \quad \textbf{(12)}$$

Substituting for *iLB,*peak given in (3) and using (11), the average input current is given by

$$I_{\text{in}} = \frac{V_{\text{in}} + (N_3/N_1)V_{CB} - V_{Ca}}{2L_B} d^2 T_S \times \left(\frac{(1 + N_3/N_1)V_{CB} - V_{Ca}}{V_{CB} - V_{\text{in}}} \right). \quad (13)$$

Based on (13) for a given input voltage, Fig. 6(a) shows the normalized input current waveform in a half cycle for a change in the turns ratio *N3/N*1 . It can be seen that to reduce the dead time and improve the power factor of the input current the turns ratio must be ≥0.5. Similarly, Fig. 6(b) shows the normalized input current waveform for a change in dc bus capacitor voltage *VCB*. As it can be seen that the higher the *VCB* the better quality of the input current waveform (lower THD). However, higher *VCB* means higher voltage stress on the power switch (SW),which can reduce the efficiency of the converter. Therefore, a tradeoff between THD and efficiency must be made.

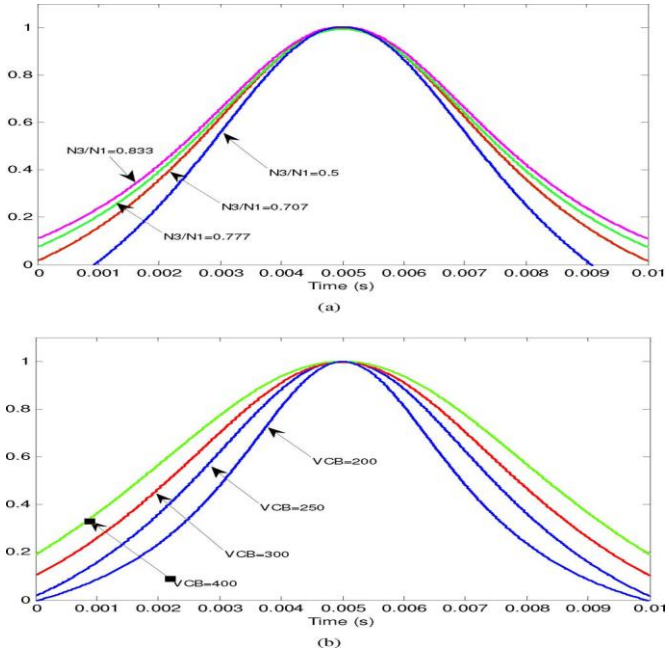
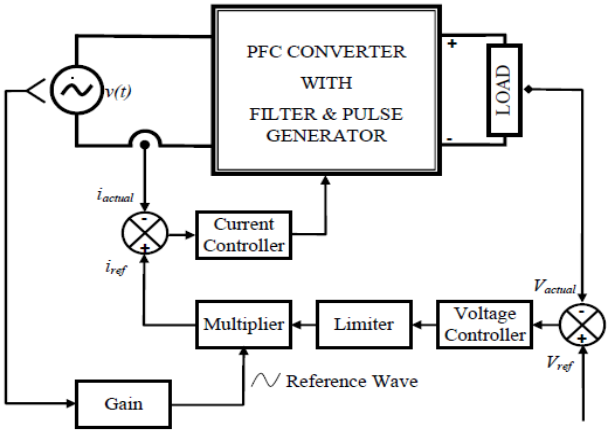


Fig: (6). Normalized input current waveform in half cycle for a change in (a) turns ratio N3/N1 (b) bud capacitor voltage VCB.

III. CLOSED LOOP CONTROL of ACTIVE PFC CIRCUIT



Fig(7) Closed Loop Control for PFC ac-dc Converter

The general block diagram of the closed loop control of PFC converter is shown in Fig:7. The objective is to regulate the power flow and meet the UPD input performance index such as output voltage regulation ≤ 2%, input power factor ≥ 0.95, input current distortion THD ≤ 5%. The output voltage is regulated by the outer voltage control loop. The

input power factor and current wave shape are controlled by the inner current loop. Both controller are chosen as PI type compensator and represented by the transfer function Gc(s) = Kp(1+1/Ti s). Where Kp and Ti are proportional gain and integral time constant respectively. The output voltage is regulated using voltage error (Verror) obtained by comparing the measured actual output voltage (Vactual) and desired reference voltage (Vref). The Verror is processed by the voltage PI-controller whose output is the desired current magnitude and limited to a designed maximum value. It is multiplied with unity magnitude sine-wave reference derived from input voltage. The output of the multiplier is the desired sinusoidal input reference current signal (iref) with magnitude and phase angle. This signal is further processed by the linear current controller as detailed in Fig. and generates pulse width modulated gate pulses such that converter maintain input performance index.

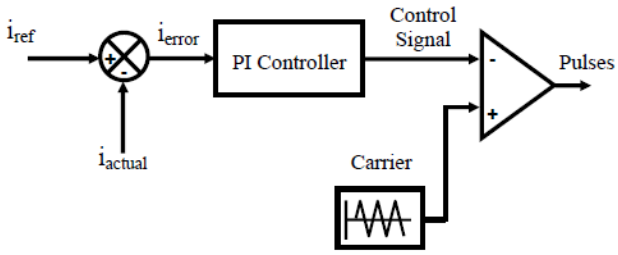


Fig:8. Linear current control

The outer/voltage loop controller parameter values for Kp and Ti are designed to maintain constant output voltage irrespective of disturbance due to change in load/ input voltage. Kp and Ti are found from open loop converter output voltage response for a step load change [5]. Whereas the inner /current loop controller values for Kp and Ti are designed to optimize PWM pulses such that converter operation maintains input current near sinusoidal with limited distortion and power factor near unity.

IV. MATLAB/SIMULINK MODEL and SIMULATION RESULTS

Here simulation is carried out for two cases in Case 1 AC to DC conversion without APFC is presented and in Case 2 with APFC is presented.

AC to DC Converter Without APFC

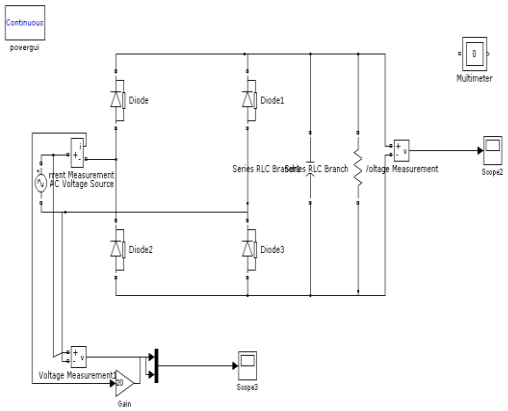


Fig.9. Matlab/Simulink Model without APFC

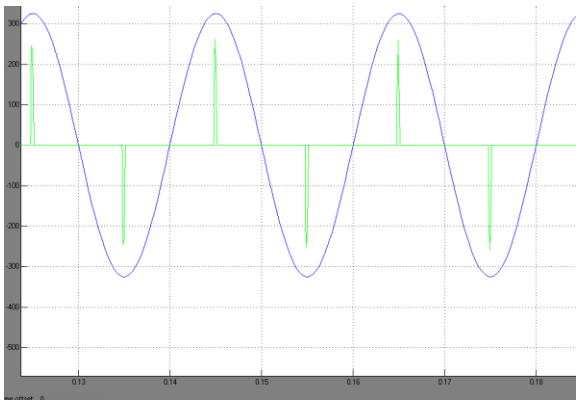


Fig.10: AC side voltage and current waveforms without APFC.

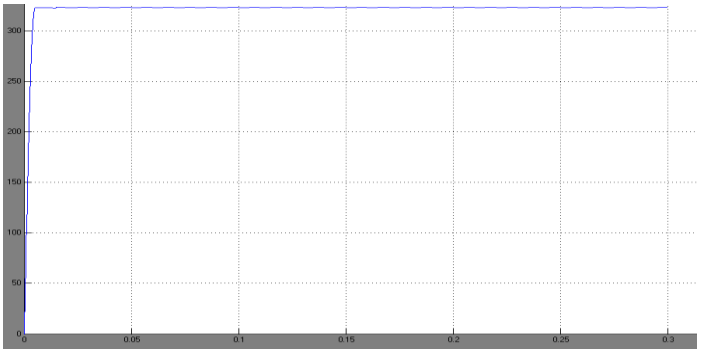
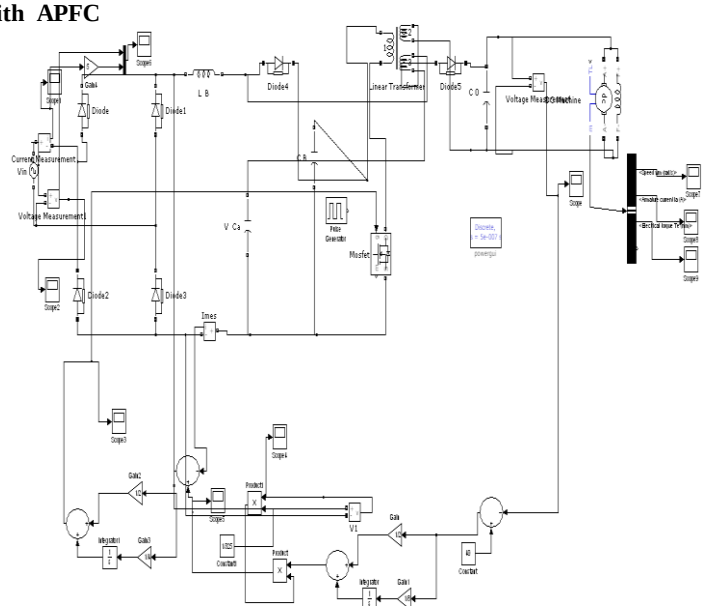


Fig.11. Output DC voltage

AC to DC Converter With APFC



Fig(12)Matlab/Simulink Model with APFC

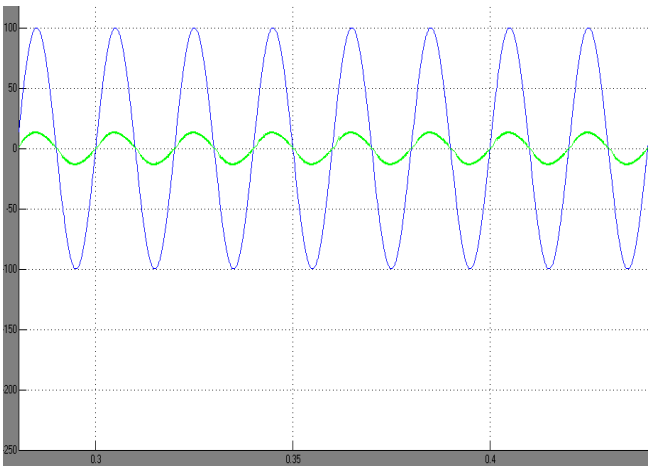


Fig.13: AC side voltage and current waveforms with APFC.

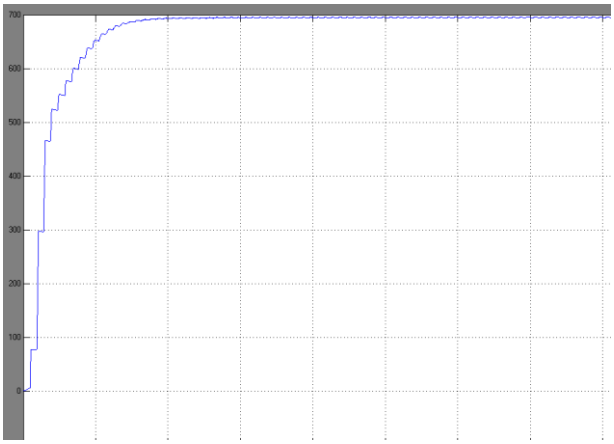
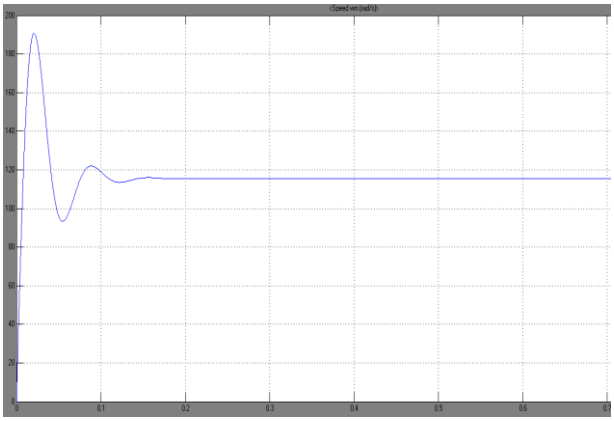


Fig.14: Output DC voltage



Fig(15) DC motor speed in rad/sec

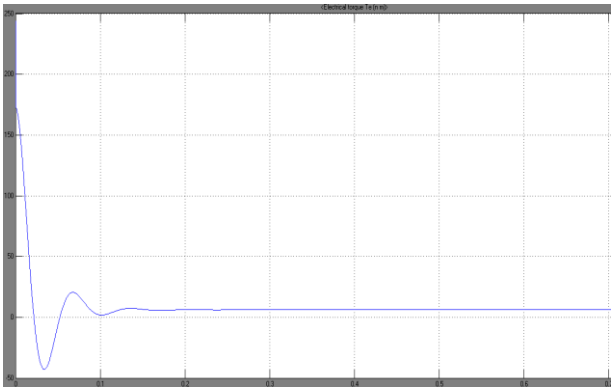


Fig.16: DC motor Torque in N-m

V. CONCLUSION

In this paper, a new ac/dc converter based on a quasi-active PFC scheme has been presented. The proposed method produces a current with low harmonic content to meet the standard specifications as well as high efficiency. This circuit is based on adding an auxiliary winding to the transformer of a cascade dc/dc DCM flyback converter. The proposed converter is applied to a dc motor drive. Finally a Matlab/Simulink based model is developed and simulation results are presented.

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